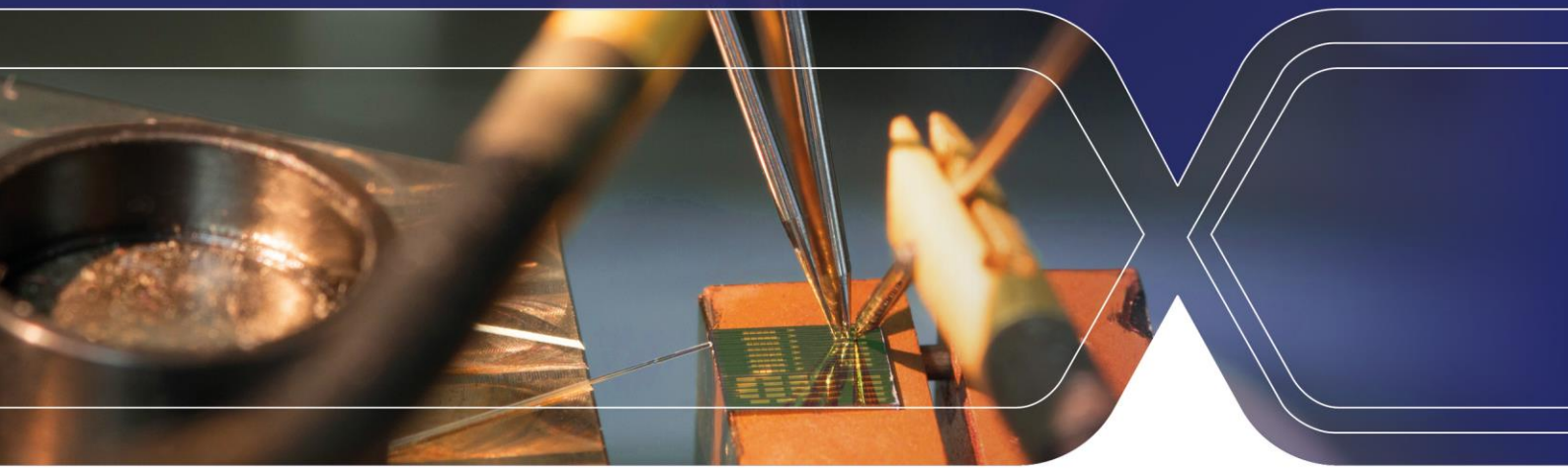

Design-Agnostic PIC Validation

Application specific photonic integrated circuits (ASPICs) state an appealing solution for emerging fields in photonic integration, such as quantum technology. Already deployed in telecommunication, biophotonics, sensing and signal-processing applications, ASPICs are featured by small foot-print, low-weight and low-price.

For quality assurance, every fabricated wafer needs to be validated. To avoid time-consuming and expensive characterization of individual designs, dedicated test structures are present on fixed positions on each wafer, allowing user design-agnostic platform validation. Smart testing routines reveal the performance of the most crucial photonic building blocks.

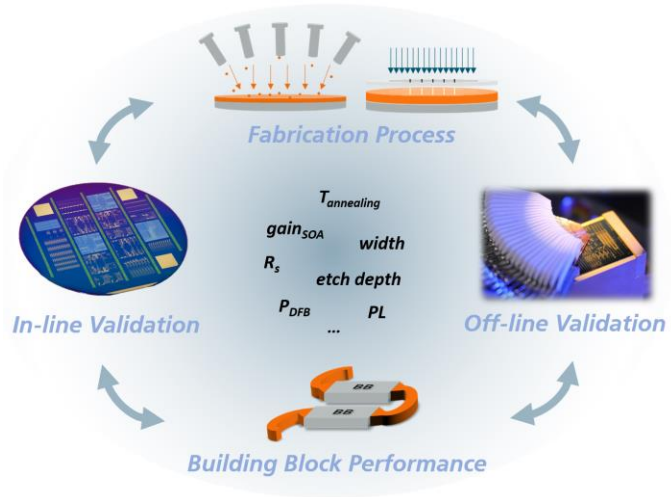

Figure 1: Wafer validation cells (blue area) and PCM structures (green area) on an InP wafer with dependencies to fabrication process and BB performance

Semiconductor manufacturing, and especially in the Foundry – Design House business model, separates the processing technology from the PIC functional design, in such a way that one qualified technology (process) is used to manufacture a wide range of products (designs). The designer accesses the processing technology through a Process Development Kit (PDK). Given the complexity of semiconductor manufacturing, this has proven to be a key element for success, as yield learning from a product can be easily propagated throughout the entire technology, while development and maintenance resources are used efficiently.

Technology Development & Product Development are therefore separated, leading further to a separation of quality control during manufacturing. Wafer Validation is ensured by the Foundry quality control, through the means of design agnostic Process Control Modules (PCMs), consisting of technology elements measured either during inline processing (e.g.: step height measurements, optical critical dimension measurements) or electrical tests (e.g.: metal sheet resistances, capacitances, isolations etc.) as well as building block / PDK elements tests (e.g.: photodiode dark current, DBR laser threshold current, modulator V_π etc.).

Technology Characterization & Qualification vs. Wafer Validation

During the ***Technology Development*** phase, the Foundry characterizes the PDK elements (Devices / Building Blocks) and shares the relevant data with the designer, through the means of graphs, tables and compact models. In addition, it also qualifies the technology by running a number of wafers & ensuring each of them passes the Wafer Validation and by performing reliability tests (Device reliability & Reference/Leading Product Reliability).

During the ***Product Development*** phase, the designer validates together with the Foundry that the design can be manufactured in the technology used for processing regarding functional performance & yield and qualifies the product. Usually, a first "leading" product is needed to fully qualify a Technology. This may be replaced by reference designs / IPs.

During the ***Manufacturing*** phase, the Foundry performs a series of inline measurements & **tests** to assess the quality of **every wafer**. These are significantly less extensive than the full characterization and qualification done in the development phase. They are designed to capture a relevant footprint of the technology and ensure that the processing and its results are within the boundaries of the material used for qualification & PDK. The elements needed for the Wafer Validation are extracted from the Process & Building Block Failure Mode and Effects Analysis (FMEAs). When certain elements of an FMEA cannot be detected through the metrology & test performed on each production wafer, periodic characterization or reliability tests may need to be set up to ensure that quality is monitored and controlled.

Characterization is mainly used to offer insights in the device performance and to extract the relevant information needed to design. It is an attribute of the **development** phase. It mainly consists of curves requiring engineering interpretation.

Tests are used to ***Validate each Wafer*** (Pass/Fail) and statistically monitor the process. It is an attribute of the **manufacturing** phase. Tests are a consequence of FMEAs and developed using the knowledge acquired with **Characterization**. They are often subsets of a characterization measurement, e.g., one or a limited number of points from a characterization curve). They consists of parametric data (one value per measurement), judged through the means of upper & lower specification limits.

Wafer Validation Strategy Development

Development of a Wafer Validation Strategy for a specific technology comprises the following:

- Definition of the **Critical to Quality** elements, that need to be checked / monitored to ensure

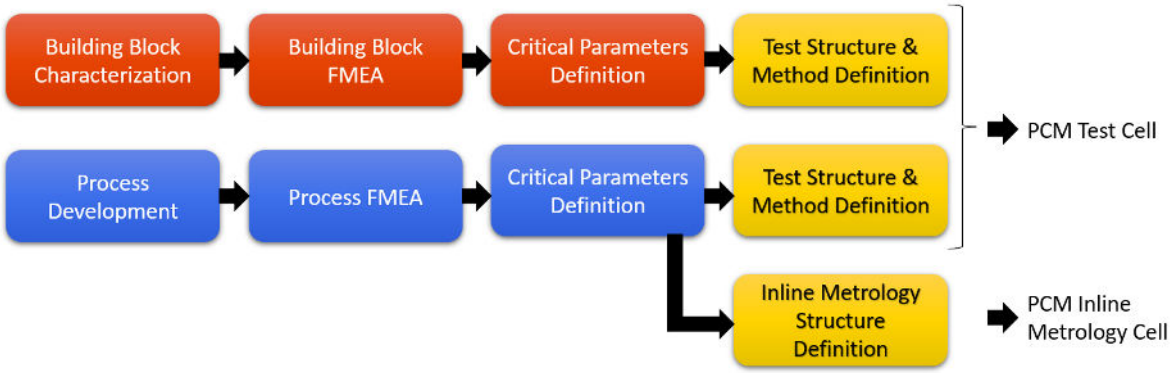

Figure 2: Wafer Validation Strategy Development

that the process is under control & giving the correct output from a design point of view (these are results of the Process & Building Block FMEAs)

- Definition of **Process Control Monitoring (PCM) Cells** on which the metrology & test can be performed. These cells are to be added to each design.
- **Parametrization** of each measurement (reducing each characteristic to a value with a label called “parameter”)
- **Ranking** of each parameter (from critical to informative; various ranking schemes can be applied).

Figure 3: Parameter Ranking Example

- Setting up **Targets & Functional Specifications** for each parameter (low ranking / informative parameters may not have specifications). These come in the form of **LSL** (lower spec limit) and **USL** (upper spec limit). An additional set of limits (control limits) may be specified. It is not used for Wafer Validation, but for Statistical Process Control. Its purpose is not to identify functional violations, but rather process drift and, thus, prevent functional violation before it appears.
- Setting the **Wafer Disposition Criteria,** to define on how many sites (positions) a parameter is to be measured, the conditions under which it is considered a PASS or a FAIL, and the actions to be taken in each case. For example, a standard Prio1 parameter may be measured on 5 sites, with a PASS when at least 4/5 sites are within specs. A fail can trigger a rework, or a scrap, depending on the situation. A more critical Prio1 parameter, also measured on 5 sites, may only PASS when all 5 sites are within specs. 4/5 may trigger a re-measurement on all available sites with PASS if no other site fails.

Wafer Validation Process

During manufacturing of each wafer, inline measurements are made after each critical step. At the end of the flow, an on-wafer electrical test is performed. In typical production scenario, a subset of PCM cells, spread evenly across the wafer, are measured.

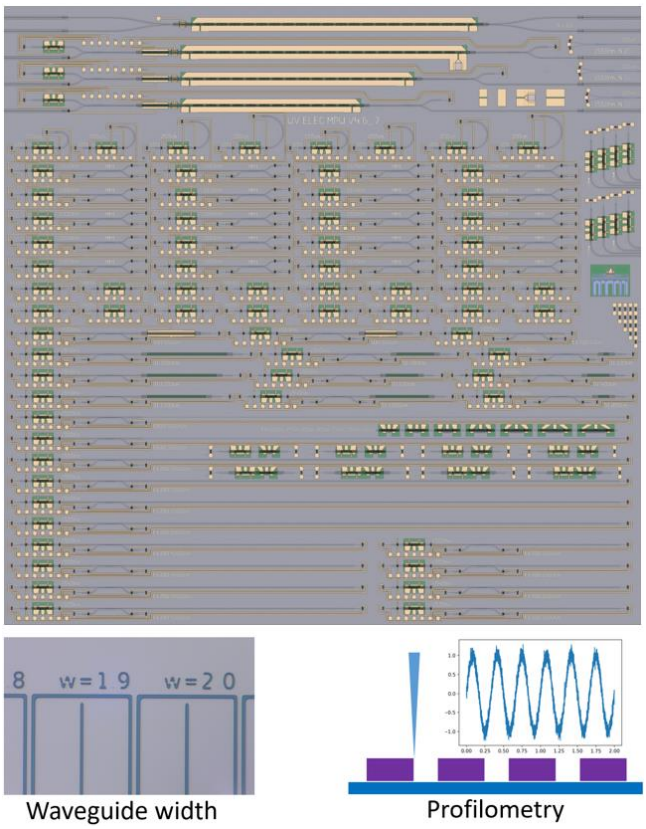

Figure 4: Wafer validation cell and PCM structure

Parameters can be directly measured, derived from multiple parameters or extracted from a characterization curve using a specific algorithm.

Each parameter will have a value for each site of the wafer and will be checked with respect to the limits (USL, LSL).

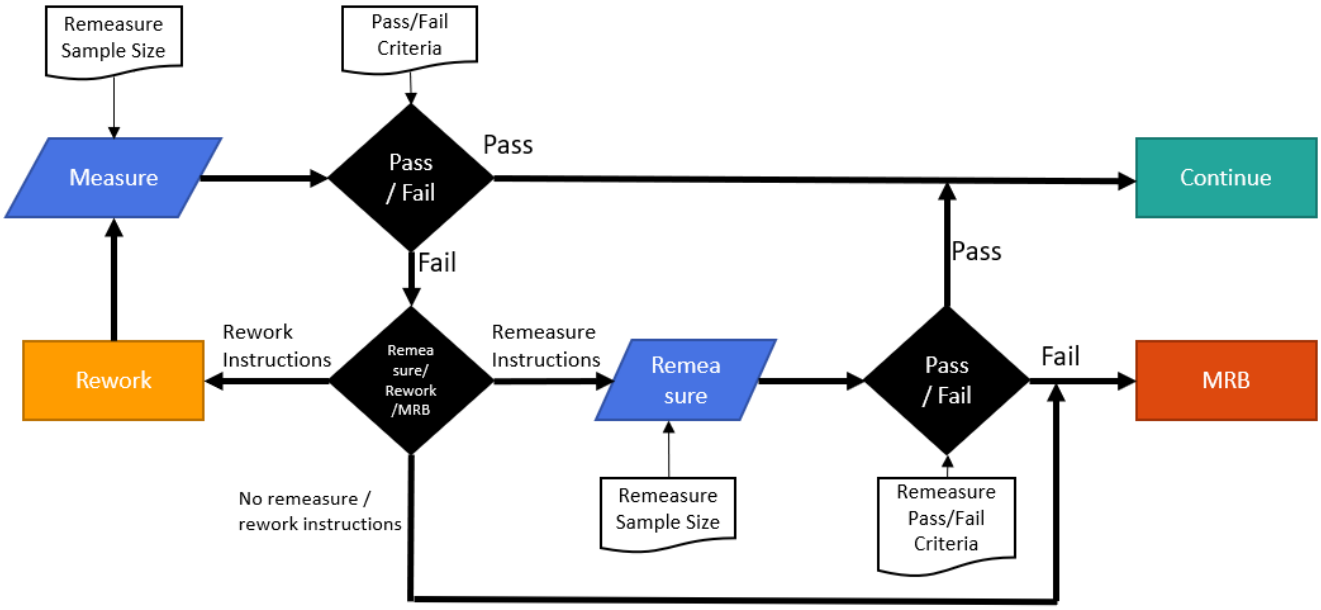

Figure 5: Wafer Disposition Flow

In case of a failure of a parameter that is part of the Wafer Acceptance Test (WAT), when no rework is possible and qualified, the wafer is passed through an MRB (Material Review Board) which decides:

- What happens with the material: scrap, waive or nonstandard rework. This is done in accordance with internal quality criteria & customer agreements.
- What additional actions need to be taken, such as: inform customer, start root-cause analysis, start additional wafers

Example

WVG_ADI_CDB_Line-2000: parameter linked to the measurement of the width of waveguides after photoresist development, using a CD-SEM equipment on the Inline PCM cell that was added to the mask design; it has an LSL=1800nm and USL=2200nm.

The measurement was carried out on 14 positions, out of which 3 gave results above 2200nm. The measurement is a fail and a rework procedure (that involves stripping the photoresist and restarting the lithography process) is initiated.

After the rework, all 14 positions are within specs. The result is PASS and the wafer continues to the next step.

Wafer Verification Document

A summary of the Wafer Acceptance Test results is provided in the form of a Wafer Verification Document (WVD), attesting the quality of the material before shipment.

In addition to the general specs exemplarily given in Figure 6, pilot line customers are able to extend the list of parameters against which the process is validated.

component	parameter	typical value	pass criterium
waveguide			
	propagation loss (E200, E600 and E1700)	2 dB/cm	<= 5 dB/cm
butt-joint			
	loss	2 dB	<= 5 dB
photodetector			
	responsivity, including coupling via SSC	0.5 A/W	>= 0.3 A/W
spot size converter			
	coupling loss to SSMF	1.5 dB	<= 4 dB
DFB laser			
	power @ 50 mA	3 dBm	>= 0 dBm
	wavelength accuracy @ 50 mA	<= ±4 nm	<= ±8 nm
	series resistance	12 Ω	<= 20 Ω
SOA			
	gain @ 900 µm, 100 mA	10 dB	>= 5 dB

Figure 6: Wafer Validation Specification

In case of failures that were judged as no scrap, a waiver is required from the customer and attached to the WVD.