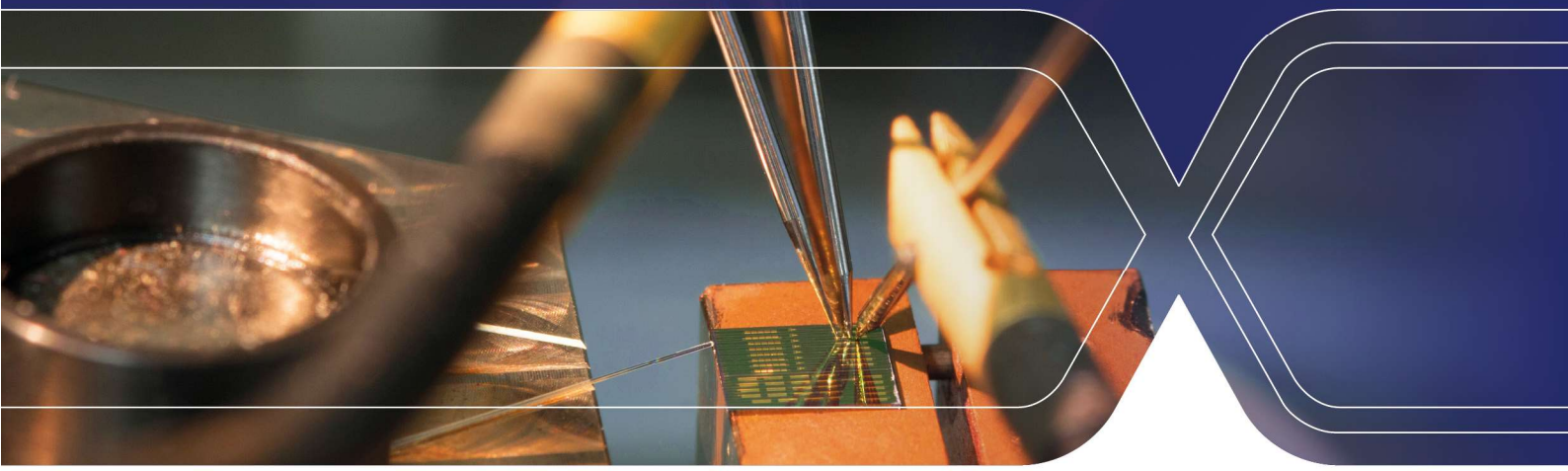

Integrated photonic circuits technology

Photonic integration has evolved from integrating single optical devices and functionalities to large scale integration of 10s to 100s of functions, forming photonic integrated circuits (PICs), much alike integrated circuits (ICs) in microelectronics[1]. PICs rely on the fact that light can be guided in waveguides. Making use of thermal and electro-optic phenomena, phase and amplitude modulation of the optical signals can be achieved. The most common material platforms for PIC fabrication are silicon nitride (SiN), silicon-on-insulator (SOI), and indium-phosphide (InP)[2]. The following table summarizes some of their main attributes:

InP	*SOI*	*SiN*
Most mature	*Smallest size*	*Lowest loss*
Best for lasers and actives integration	*Best for e/o integration*	*Best for long waveguides*
1.3-1.7µm	*1.1 - 3.7µm*	*0.5 - 3.7µm*
high cost per mm²	*challenging to get light in/out*	*No actives, no e/o integration*

Nowadays, sophisticated PICs can combine 100s of components on a single chip, including lasers, modulators, detectors, amplifiers, filters and more[3].

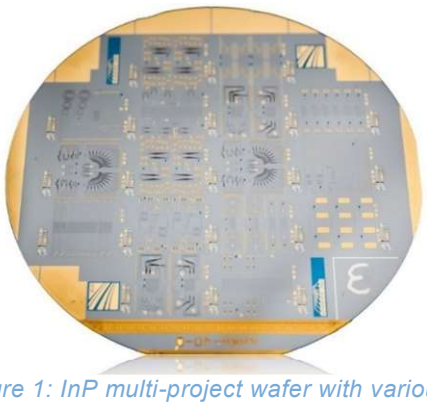

Figure 1: InP multi-project wafer with various PIC designs and projects from HHI.

Open access PIC fabrication in Europe

Similar to what happened with electronic ICs, volume production of PICs requires highly specialized and capital-intensive manufacturing infrastructure. The open-access foundry model offers PIC manufacturing services to external users, lowering investment for fabless companies and PIC-based product development. Foundries provide a generic integration platform, which gives access to their standardized fabrication platforms and provides a set of predefined building blocks in form of a Process Design Kit (PDK).[4] Basic building blocks (BBBs) like waveguides, amplifiers, detectors, and phase modulators can be assembled into composite building blocks (CBBs), like Mach–Zehnder switches or lasers, and thus provide the basis for complex PIC design on a functional level. The design flow is accelerated by using BBBs with stable and reproducible performance available in

[1] https://doi.org/10.1103/RevModPhys.49.361
[2] "Generic integration technology and JePPIX InP foundry platform" OFC, 2018
[3] https://doi.org/10.1049/el.2014.2011
[4] https://doi.org/10.1109/JSTQE.2017.2720967

integrated design software solutions offered by third party vendors. This PIC manufacturing flow has led to a whole ecosystem offering software tools, design support, packaging, testing and assembly services for PIC-based products.

MPWs: From ideas to prototypes

In the earlier stages of product development, multi-project wafer (MPW) runs allow users to efficiently test their design ideas using the standard process flow. Multiple users share the design wafer area and thus the fabrication costs. Figure 1 shows such a multi-project wafer. Mask designs are kept confidential to ensure protection of each user's IP. Each MPW run participant will receive a few chips, which they can evaluate themselves or have tested through a third party service. For more design space, dedicated runs are available as well.

Pilot Line: From prototype to pilot production

Currently, the fixed process of an MPW enables proof-of-concept and prototype-level research. The transition to pre-commercial product maturity might still involve design adaptations and streamlining of activities towards a validated module, including, e.g., testing and packaging. This imposes yet another significant cost-barrier in the product development cycle. A pilot line supports this transition. Efforts include the standardization of processes, PDKs, testing, and information flow along the supply chain. Companies can benefit from the reduced barrier-to-entry and the alignment towards a seamless value chain from design to fabrication (Fig.2), taking their product prototype towards pilot production.

Open access workflow

The workflow in the open access ecosystem usually starts with a platform 'broker': JePPIX is the access point to the ecosystem and offers support to the user by, e.g., coordinating MPW inquiries and design submissions as well as access to PDKs, design support and tools. Initially, a user needs to determine if the InP PIC technology can meet the specifications of the targeted application. Experienced companies within the ecosystem can offer support for every

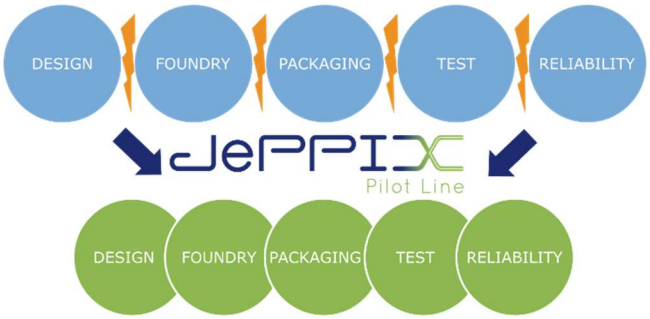

Figure 2: Connectiong all the elements of the PIC supply chain, ensuring quality control from design software through to known-good-die.

stage of the PIC product development cycle. Once the feasibility is determined, the most suitable foundry for this project needs to be selected. The product design team can then make use of the foundry-specific PDK to design their (sub-)circuits or begin designing custom building blocks based on the technology handbook and design rules for the selected fabrication technology. Software suppliers complete the toolset for PIC designers, offering component to circuit to system level simulation, including layout generation and verification. The design can be optimized over multiple tape-out iterations making use of MPW runs, typically offered four times a year. Concept validation and prototype verification can be done by the user or contracted out. Scaling the prototype to pre-production levels will also need to include packaging, testing and reliability insurance processes. This is where the JePPIX Pilot Line aims to make impact: streamlined designs and technology standards developed throughout this and other pilot line projects aim at a tighter cooperation between the industrial players in the value chain. Enabling users to innovate for themselves with state-of-the-art design and test tools in a fabless and labless environment.

Discuss your application with us

If you are interested in knowing more about the capabilities and use of InP PIC technology or the JePPIX Pilot Line project efforts and its offer, contact JePPIX. The JePPIX Pilot Line (pilotline@jeppix.eu) provides low entrance-threshold to mature-manufacturing, taking open access InP PICs from proof of concept to industrial prototyping levels.