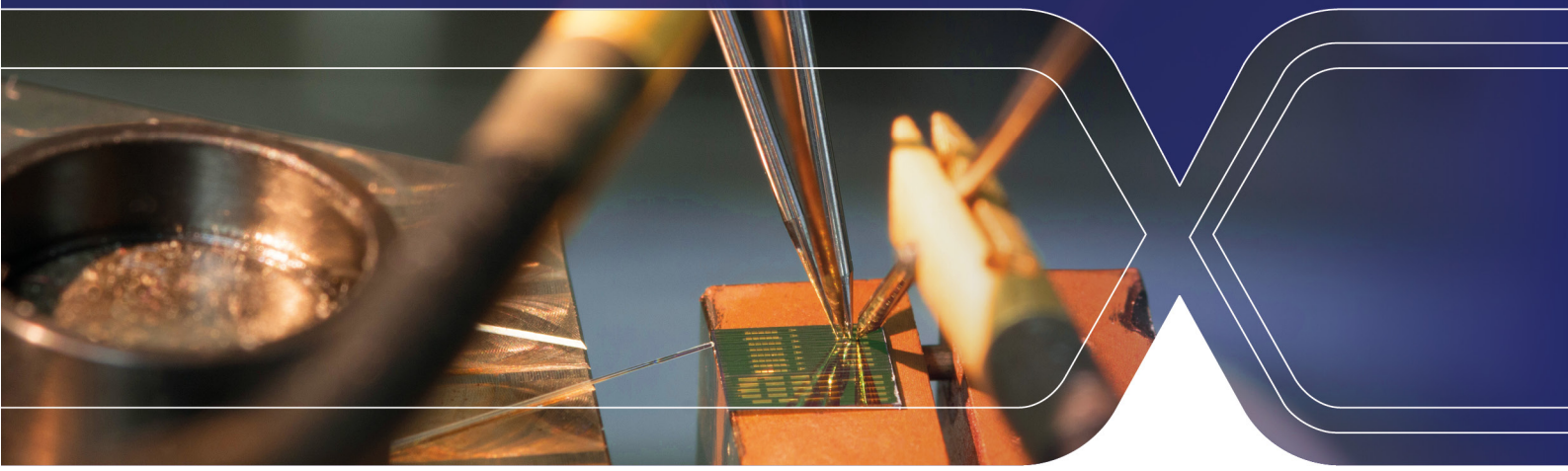
Technical Note
InP Lasers for Hybrid PICs

JePPIX
Platform for Photonic Integration



Hybrid Photonic Integration

Photonic integration offers the exploitation of photonic functions on a chip, reducing mass, size and cost per piece. Various integration platforms are being explored and developed for photonic integrated circuits (PICs), with silicon-on-insulator (SOI), silicon nitride (SiN) and indium phosphide (InP) representing the major material platforms currently used. All three platforms are nowadays easily accessible through multi-project wafer (MPW) runs offered by specialized foundries, allowing for cost-effective product development. Each of these technologies has its own competitive strengths and shortcomings. Increasingly, efforts in research and development target to harvest of the best of each technology by combining two different materials or platforms in hybrid or heterogeneous integration schemes. The table below provides a rough qualitative overview for orientation of these integration approaches. InP, the only direct bandgap material in this overview, is the platform of choice for active photonic devices, including tunable and narrow-linewidth lasers, amplifiers and high performing modulators. The SOI platform offers the highest integration density out of these technologies and offers well-performing passive devices as well as high-speed modulators. The SiN platform, on the other hand, is a purely passive integration platform, offering optical modulation only through thermal effects. The extremely low loss and low susceptibility to phase errors are the competitive edge of this integration platform[1]. In combination, these platforms can offer optimized performance, while simultaneously lowering cost, size and power requirements[2]. The main challenges associated with hybrid photonic integration are the complex alignment processes and the requirement for more sophisticated assembly processes. While challenging, commercial products have been realized and steady progress is reported[2,3].

Table: Qualitative overview of the strengths and weaknesses of the main integration PIC platforms, taken from [4].

	InP	*SOI*	*SiN*	*Hybrid*
strength	*most mature*	*smallest size*	*lowest loss*	*optimized performance and integration cost*[5]
lasers	✓✓✓	x	x	✓✓✓
modulators	✓✓	✓	x	✓✓
photodiodes	✓✓✓	✓✓	x	✓✓✓
passive building blocks	✓	✓✓	✓✓✓	✓✓✓

[1] https://doi.org/10.1109/JLT.2020.2972065
[2] https://doi.org/10.3390/app9081588
[3] phastflex.jeppix.eu
[4] https://doi.org/10.1088/2040-8986/abc312
[5] https://smartphotonics.nl/silicon-photonics/

Hybrid Integration Approaches

Hybrid photonic integration, particularly integration of III-V semiconductor opto-electronic components, can be realized with various approaches. These include butt-coupled individual chips, flip-chip integration, bonding approaches, or hetero-epitaxial growth[6]. Out of these options, butt-coupling and flip-chip integration allow individual processing of the photonic chips. This has the advantage that device fabrication is performed on its native substrate, not compromising performance through adapted processes and additionally allowing for known-good-die selection of the involved PIC modules.

Butt-coupled hybrid integration is straightforward and is typically achieved by aligning all six degrees of freedom and connecting the two chips with index matching glue for permanent coupling. This approach is illustrated in Figure 1, where InP-based gain sections were combined with low-loss SiN waveguides and micro-ring resonators to realize a narrow-linewidth integrated laser[7]. The approach has shown well-performing devices, but limits coupling to the chips' edges, making this approach incompatible with wafer-scale integration.

A more sophisticated approach, compatible with wafer-scale integration, is flip-chip integration. Flip-chip integration strategies can be classified into two types: edge coupling, and surface coupling. Figure 2 illustrates some of the most common types of flip-chip integration of InP PICs with other PIC platforms[2]. Hybrid integration by means of edge coupling does benefit from deeply etched waveguide terminations (i.e., etched facets) compared to cleaved-waveguide facets[2]. The latter allow typically ±10 µm accuracy in I/O interface positioning. Deeply etched waveguide terminations can reduce this to sub-micron levels. Additionally, back reflections can be controlled better by introducing an angle between waveguide and etched facet and optical coatings can be applied on wafer-scale.

Other strategies shown in Figure 2 use vertical coupling schemes. These are not only attractive for flip-chip hybrid integration allowing for coupling at virtually any position without prior etching, cleaving and coating procedures, but also enable on-wafer characterization and testing. The depicted surface coupling schemes utilize grating couplers and vertical mirrors.

With hybridization gaining in popularity across various application fields, the here presented I/O interface options and integration schemes pose attractive solutions for including InP PIC-based devices on other material platforms, taking advantage of their combined strengths.

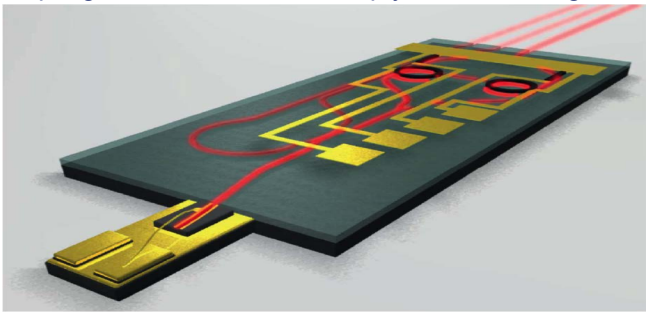


Figure 1 Illustration of a hybrid laser, with the semi-conductor amplifier on the lower left part and the SiN waveguide feedback circuit in the upper right, from [7].

Discuss your application with us

If you are interested in knowing more about the capabilities and use of InP PIC technology for hybrid integration, contact JePPIX. The JePPIX Pilot Line provides low entrance-threshold to mature-manufacturing, enabling high-TRL development in a scalable design kit driven process, taking open access InP PICs from proof of concept to industrial prototyping levels.

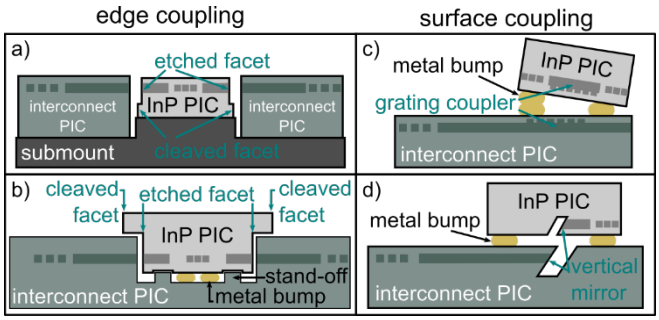


Figure 2 The four most common hybrid integration approaches separated into edge-coupling and ruface coupling strategies, adapted from [2].

[6] https://doi.org/10.3390/photonics2030969
[7] https://doi.org/10.3390/photonics7010004