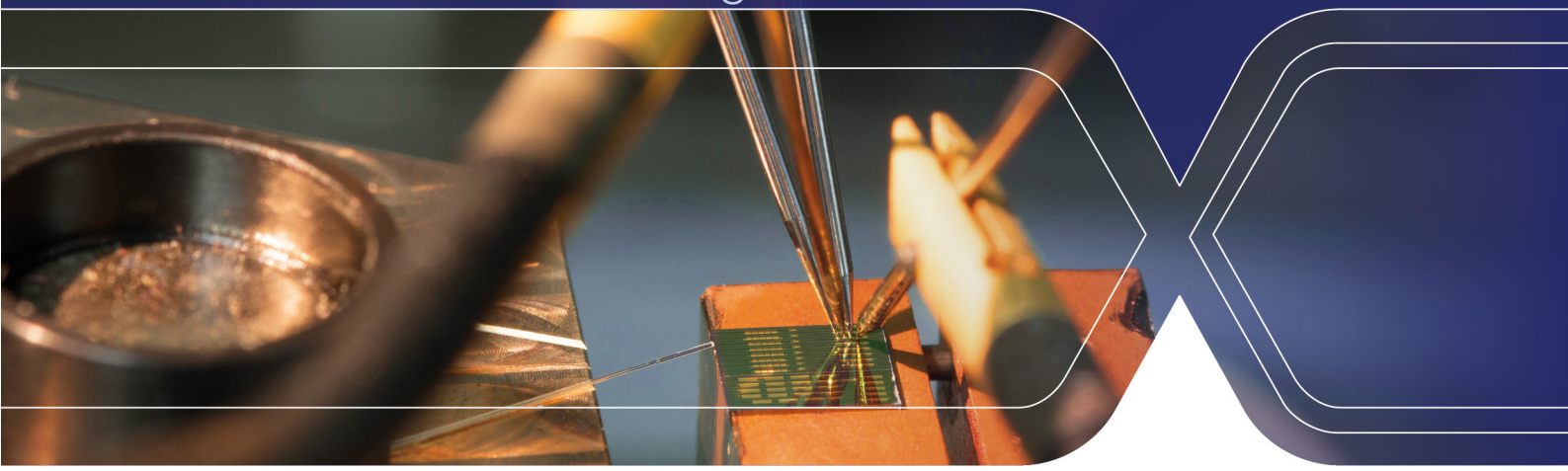
Technical Note

Automated Photonics Testing

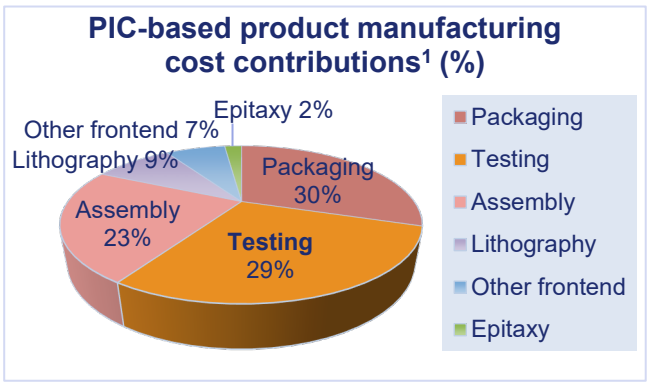
JePPIX Platform for Photonic Integration



Fully automated PIC testing

Indium phosphide (InP) photonic integrated circuits (PICs) are deployed in an increasing number of fields and applications. The JePPIX PIC ecosystem and the open-access foundry model enable fabless and lableless companies to utilize InP PIC technology for their own product development. One crucial factor in bringing these PIC-based systems and applications to the market is time-efficient PIC characterization and validation at low cost per part. Automated testing is essential to achieving this.

Testing has been identified as one of the main cost factors in PIC-based product manufacturing, together with packaging and assembly costs[1]. The reason for the high impact of testing on cost is the spread of testing activities across different stages of manufacturing. This includes, but is not limited to, process qualification, building block qualification, and circuit-level validation. Both testing and test data handling require standardization and increased levels of automation to align efforts along the PIC manufacturing supply chain[1]. Test automation is thus a substantial enabler for volume production, by reducing cost and improving scalability and yield. The JePPIX pilot line[2] supports scaling up from prototype to manufacturing readiness. This includes test-as-a-service implementation in connection with the packaging pilot line PIXAPP[3] and efforts to further develop automated, production-grade die testing tools in collaboration with ficonTEC[4,5].



Testing machines and requirements

The testing tools enable automated electrical, optical or mixed-signal electro-optical characterization of singulated and on-wafer dies. Specific to photonic devices and yet universal for PIC testing is the optical alignment process with the key performance metric of alignment time. A temporary, stable optical connection has to be established from the PIC to the testing equipment, typically using optical fibers with active feedback of in/out-coupled light. The time required for alignment has many underlying factors, which fall into three main categories: mechanical system, optical metrology and overall methodology[6]. Some important factors and the technical challenges are presented here.

[1] https://doi.org/10.1109/JSTQE.2019.2921401
[2] www.jeppix.eu/pilotline/
[3] https://pixapp.eu/
[4] https://www.ficontec.com/
[5] https://doi.org/10.1109/ICTON51198.2020.9203537
[6] https://doi.org/10.1117/12.2511039

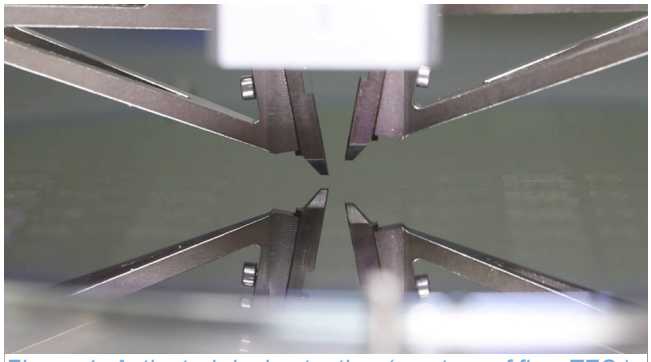


Figure 1: Activated device testing (courtesy of ficonTEC)

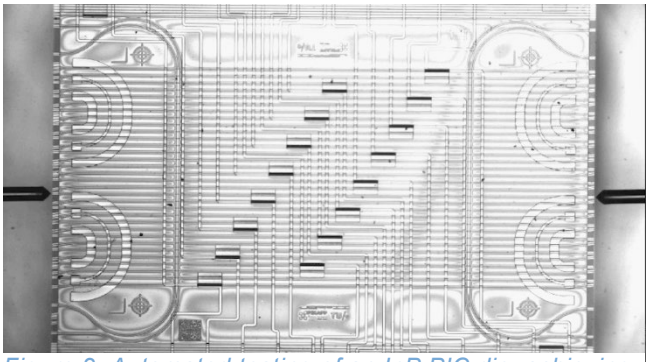


Figure 2: Automated testing of an InP PIC die, achieving dual fiber alignment in 1.7s (courtesy of ficonTEC). PIC designed by TUE and fabricated by SMART Photonics.

Mechanical system

Mechanical axis acceleration is one of the most important factors directly influencing the time for active alignment. The high accelerations achievable by modern positioning systems put stringent conditions on the fiber holder design, as bending of the fiber holder can become considerable compared to the accuracy required. Fiber holder design thus requires appropriate optimization of height, thickness, material constants, but first and foremost of its length.

Optical metrology

Optical metrology considerations for optical alignment times need to include accuracy of the pre-alignment process through image processing, beam profiling and suitable fitting, measurement noise, and the frequency of the optical power measurement. The latter is in practice limited by processing time, rather than the actual measurement time. Yet, the available processing frequency of high-speed motion controllers can only be fully exploited if the fiber holder design is adequate for the frequency. If not, the alignment time will be ultimately limited by the bend of the fiber holder, revealing the importance of appropriate fiber holder design.

InP Photonic Integrated Circuits (PICs)

Optical chips or PICs can contain tens to hundreds of optical components. While electronic integrated circuits (EICs) consist of transistors, capacitors, and resistors, a PIC consists of, for example, lasers, modulators, photodetectors, and filters, all integrated on a single substrate. Several application fields, such as data- and telecom, sensing and lidar are already using or are considering the use of PICs for their products. This PIC technology is accessible to users without a cleanroom, through so-called multi-project wafer runs and open access foundries. InP based technology is commercially available through SMART Photonics and Fraunhofer Heinrich-Hertz-Institute. Access is individually coordinated by JePPIX.

Overall methodology

The overall methodology captures the alignment aspects of first light strategy, alignment algorithm and its calculation time, and parallelization by using fiber or periscope arrays. Simultaneous alignment of several channels can efficiently reduce the time per tested part, reducing not only alignment time, but allowing parallelization of entire test procedures. For the outlook towards wafer-scale testing for InP PICs, recently developed periscopes[7] and a method relying on total internal reflection[8] enable test automation for edge coupling at wafer level. Test machine design remains a highly complex subject influenced by PIC design, application, and budget.

Discuss your application with us

If you are interested to know more about automated testing of InP PICs, please contact JePPIX. The JePPIX Pilot Line provides low entrance-threshold to mature-manufacturing, enabling high-TRL development in a scalable design kit driven process. Commercial and academic partners combine high degrees of practical experience and PIC specific knowledge to design PIC testing tools with increasing levels of automation and introduction of standards.

[7] www.vanguard-photonics.com/project/micro-lenses/

[8] https://doi.org/10.1364/OFC.2018.M3F.2