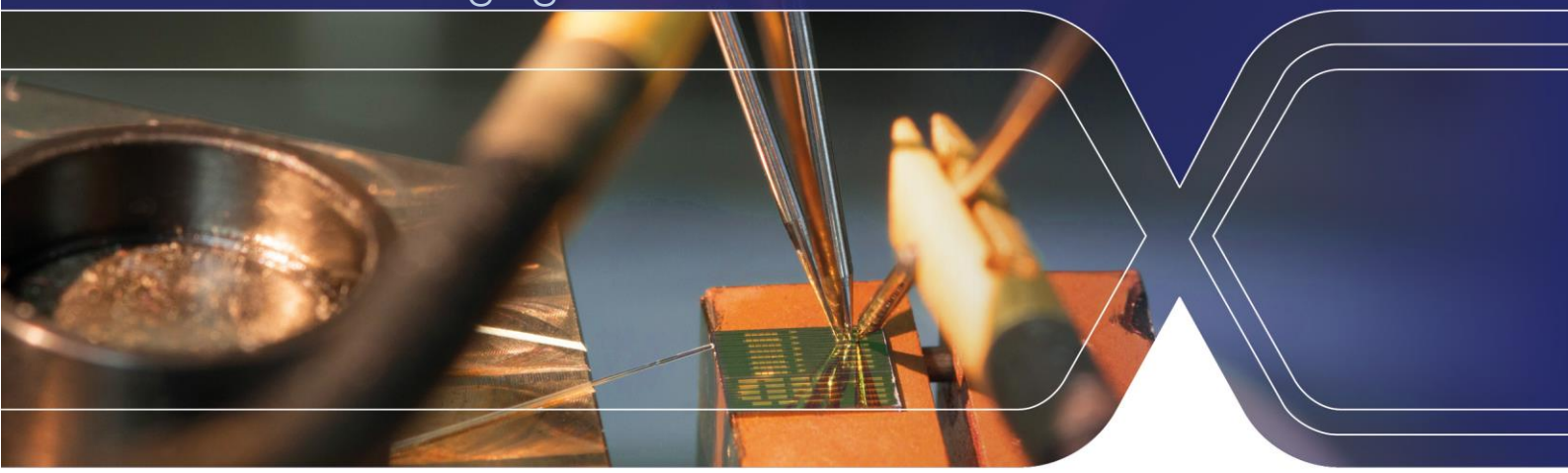
Technical Note

Photonic Packaging of InP PICs

JePPIX Platform for Photonic Integration



Photonics packaging

Photonics packaging covers the optical, electronic, and thermal coupling of photonic integrated circuits (PICs) to the outside world resorting to a suitable mechanical solution. The procedures associated with packaging of photonic devices are often underestimated and remain technically challenging. To ensure that PICs can be packaged efficiently and reproducibly, packaging specialists from the PIXAPP consortium have developed photonics packaging design rules (PDRs). These design rules specify the acceptable dimensions and locations of optical and electronic input or output ports on a PIC with respect to the physical footprint of the PIC die.

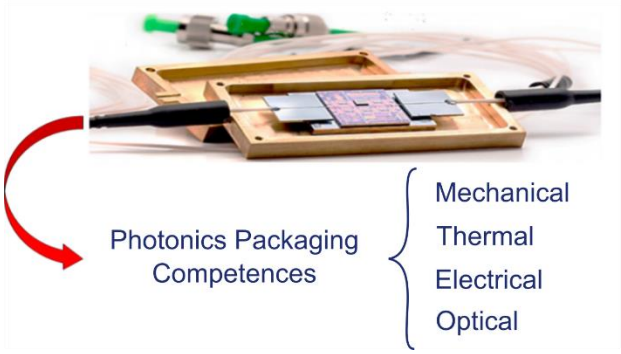


Figure: Photonics Packaging

What is packaging?

Photonic packaging is the catch-all term used to describe the range of techniques and technical competences needed to make the optical, electrical, thermal, mechanical (and sometimes chemical) connections between a PIC and the outside world.

InP Photonic Integrated Circuits (PICs)

Optical chips or PICs can contain tens to hundreds of optical components. While electronic integrated circuits (EICs) consist of transistors, capacitors, and resistors, a PIC consists of, for example, lasers, modulators, photodetectors, and filters, all integrated on a single substrate. Several application fields, such as data- and telecom, sensing, and lidar are already using or are considering the use of PICs for their products. This PIC technology is accessible to users without a cleanroom, through so-called multi-project wafer runs and open access foundries. InP based technology is commercially available through SMART Photonics and Fraunhofer Heinrich-Hertz-Institut. Access is individually coordinated by JePPIX.

While satisfying any one of these photonic packaging requirements can be trivial, especially with the tools and resources available in a laboratory environment, they can be complex to realize in high volume for products that are destined for market.

How to get this done

To facilitate clear discussions with the user, we define a compass-coordinate system to unambiguously label each side of the PIC die. We can provide packaging solutions to all standard PIC dies, provided PDRs are correctly followed. In all cases, it is recommended to review your design with your chosen packaging partner before submission to a foundry.

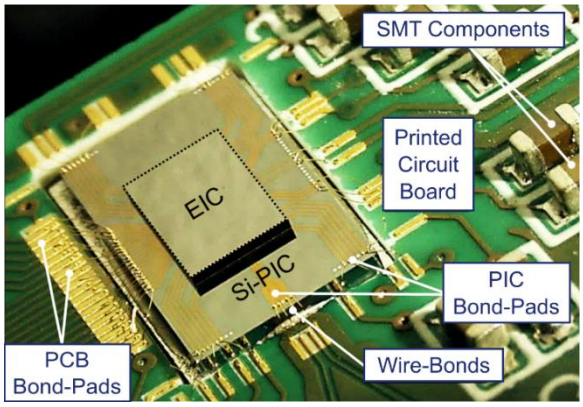


Figure: EIC integrated on top of a PIC and wire-bonded to a printed circuit board (PCB) with electronics.

In general, the user should design the optical and electrical interface of their PIC according to the layout outlined in the compass-coordinate system. This layout provides the user with the option of using generic packaging solutions that can be more cost-effective with reduced development times. It is advised to designate one side of the PIC for the optical interface (typically referred to as the west side). In this context, optical interfaces include:

- single-lensed fiber edge coupling;
- single or arrayed fiber edge coupling;
- single or arrayed fiber grating coupling.

Electrical interfaces include:

- gold ball bonds from PIC to PCB or Ceramic;
- ribbon bonds from PIC to PCB or Ceramic;
- wedge bonds from PIC to PCB or Ceramic;

If more than one optical interface is required, this should be at the opposite side of the PIC (typically the east side) to facilitate parallel optical alignment using standard techniques and equipment.

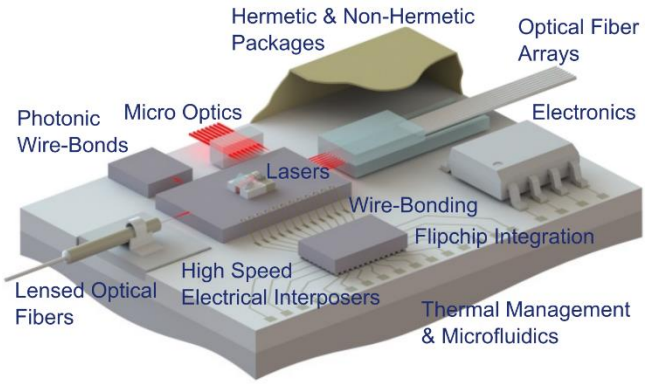


Figure: Schematic of a PIC packaged with a multi-channel fiber-array, a hybrid-integrated laser source with micro-optics, and an EIC.

Some of the involved packaging specialists contributing to both projects, PIXAPP (https://pixapp.eu/) and the JePPIX Pilot Line (www.jeppix.eu/pilotline):

Figure: Packaging equipment (Technobis): fully automated wire bonder and die bonder in use[2,3].

Current challenges

The development of standardized PDRs allow for a more streamlined transition from PIC design to packaged PIC prototype. However, to harness the full commercial potential of PIC technology there is a need to move beyond the current bottleneck in PIC packaging to large-scale manufacturing. The challenges associated with this are considerable, requiring a diverse range of advanced capabilities that are distributed across some of the European leading research institutes[1] and companies specialized on assembly, packaging[2], and machines[3]. The Photonic Integrated Circuit Assembly and Packaging Pilot line (PIXAPP), led from the Gateway at the Tyndall National Institute, faces these challenges by creating an inter-disciplinary coherent technology chain across Europe to establish the world's first open access PIC assembly and packaging pilot manufacturing line. These efforts bridge seamlessly to the JePPIX pilot line, aligning the PIC supply chain and bridging the "valley of death" often associated with moving from prototyping to volume fabrication.

Discuss your application with us

If you are interested to know more about the packaging of InP PICs, please contact Francesco Floris at Tyndall National Institute. Through the JePPIX pilot line and the PIXAPP Gateway, we work together to bring expertise to support end-users, helping and supporting users to successfully address their needs in realizing PIC devices.

[1] https://www.tyndall.ie/packaging
[2] https://www.technobis.com/themes/photonic-packages/
[3] https://www.ficontec.com/