The road to a multi-billion Euro market in InP-based Integrated Photonics

JePPIX ROADMAP 2012
Executive Summary .................................................................................................................. 4
Introduction: A revolution in Photonics .................................................................................. 5
Applications ................................................................................................................................ 6
The Ecosystem for Photonic Chips ......................................................................................... 7
Technology Roadmap ............................................................................................................... 8
Market Roadmap ................................................................................................................... 9
Chip Cost Roadmap .............................................................................................................. 10
R&D Roadmap .................................................................................................................... 11
Funding Roadmap .................................................................................................................. 12
Organisational Roadmap ....................................................................................................... 13
SWOT Analysis ..................................................................................................................... 14
Appendix: Market Roadmap Assumptions ............................................................................. 15

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JePPIX® is the Joint European Platform for Photonic Integration of InP-based Components and Circuits. JePPIX partners are Europe’s leading chip and module manufacturers (Oclaro, FhG-HHI, CIP), photonic CAD companies (Phoenix, Photon Design, Filarete), equipment manufacturers (ASML, Aixtron, OCP) and R&D institutes (III-V Lab, COBRA-TU/e, Cambridge University and Politecnico di Milano). COBRA is coordinating JePPIX (www.jeppix.eu).
Executive Summary

In the coming years the generic foundry approach will cause a revolution in micro and nanophotonics, just like it did in microelectronics thirty years ago. In Europe, three integration technology platforms are active for introducing the generic foundry concept for the major integration technologies in Photonics: JePPIX for InP-based monolithic integration, ePIXfab for silicon photonics, and TriPlex for low-loss dielectric waveguide technology. In this report, a roadmap for the development of generic InP-based integration technology is presented. It is a first version in a series, and will be updated and improved on a yearly basis.

In microelectronics, the MOSIS-program has been instrumental in providing low-cost access to advanced foundry processes since the late eighties, first to universities, later also to companies. By processing more than 50,000 designs it has given a great boost to the development of VLSI technology. We foresee a similar two-phase development in photonic integration. In a first phase low-cost access to advanced foundry processes is provided for R&D on integration of existing or novel sub-systems into a single chip. We expect that a large number of universities and other research institutes will be interested in making use of such a facility. This number can even be increased by creating national design support centers in a number of countries throughout Europe. Many of these R&D designs will be developed in close cooperation with companies, and a number of them will lead to commercial products, either from an existing company or a startup. This second phase will lead to a business, enabled by photonic ICs, which will exceed the 1 B€ level before 2020.

In this report the roadmap towards a multi-billion Euro market in generic InP-based Photonics is described. To make it happen the following steps have to be taken:

- Establishing a network of national design support centres throughout Europe coordinated by JePPIX
- Creating investment funds for supporting ASPIC development by small companies, and novel technology development, in a close cooperation between technology providers, academic and government research institutes.
- Close cooperation with companies, and a number of research institutes will be interested in making use of such a facility. This number can even be increased by creating national design support centers in a number of countries throughout Europe. Many of these R&D designs will be developed in close cooperation with companies, and a number of them will lead to commercial products, either from an existing company or a startup. This second phase will lead to a business, enabled by photonic ICs, which will exceed the 1 B€ level before 2020.

Although the present roadmap vision is shared in large measure by all partners in the JePPIX platform, its realization is dependent on many uncertain factors, both commercial and technological. Being an open access model to an enabling technology it will bring large benefits to a broad group of users. However an important uncertainty is the development of a proper business model in order to guarantee that sufficient funds can be made available to support the large investments that are required for development of novel technology generations with ever more performance. Here, European and national public-private funding will be important to share part of the risks.

Introduction: A revolution in Photonics

Photonics is a rapidly growing technology: LED-lighting, solar cells, displays, optical communication, optical sensors and imaging are increasingly penetrating our world. Photonics has been recognized by the European Union as a Key Enabling Technology (KET), a technology that enables a market that is many times larger than the market of the technology itself. Micro and nano-electronic integration technology is an example of a KET which has a huge impact on our modern society; it is applied almost everywhere.

Presently a number of large R&D projects are running for developing generic foundry technologies, and the infrastructure to make them accessible at low cost for a broad range of companies: design tools, component libraries, generic packaging technology and generic test equipment. This model, in which Europe is clearly leading, will reduce the entry costs for companies that want to apply Photonic ICs in their products by more than an order of magnitude. It will bring Photonic ICs (PICs) within reach for many SMEs and larger companies for which the entry costs of today’s technology are too high. In the coming years Generic Integration Technology is going to cause a revolution in the application of Photonic ICs, similar to what happened in microelectronics thirty years ago.

At present the overall global Photonics market is about 1/10th the size of the electronics market. If photonic integration technology is going to take a share of a few percent (comparable to the share of microelectronics in the electronics market) it will become a multi-billion market and enable an applications market that is many times larger.

Figure 1 Microscope photograph of a Photonic IC for pulse compression in a bio-imaging microscope. Chip size is 6x6 mm².

In 2007 a number of European key players in the field of Photonic Integration Technology started cooperation on the development of highly standardized integration processes that can be used for a broad range of different applications, similar to the approach in microelectronics. These processes are called generic integration processes, and the approach the generic foundry model.¹

The anticipated large reduction of R&D time and chip manufacturing costs will lead to a large growth of the share of Photonic ICs in the photonic components market. So far the use of PICs has been mainly restricted to specific areas in telecom core-network applications, where their specific functionality cannot be met by competing technologies. With the expected cost reductions through a generic foundry approach, they will also become competitive in high volume markets like the telecom access network, where they can be applied in the Central Office for integration of larger numbers of circuits which have to be repeated for each subscriber or group of subscribers. In future 10 Gb/s access networks they may also become competitive in the subscriber transceiver module.

When R&D and manufacturing costs drop, photonic chips will increasingly penetrate other applications. A good example is the fibre sensor market, which was over 400 M$ in 2008 with double digit annual growth figures. According to a recent GIO report it will exceed 2 B$ in 2015. A significant part of the sensor costs is in the readout unit, which contains one or more light sources, detectors and some signal processing circuitry. Here photonic ICs can replace a significant part of the existing modules and enable novel sensor principles to be exploited. Examples are various types of strain sensors, heat sensors and a variety of chemical sensors.

Optical Coherence Tomography is another potential application. Traditionally OCT is done in the 800 nm window, which is the preferred choice for retina diagnostics. For skin or blood vessel diagnostics 1550 nm is a better wavelength, because there the penetration depth is three times larger due to reduced scattering losses at this wavelength. This provides good opportunities for InP PICs in OCT equipment.

Another interesting class of devices comprises picoc and femtosecond pulse lasers. Here PICs containing mode locked lasers, optionally combined with pulse shapers, can provide small and cheap devices that can be used in widely differing applications, such as high-speed pulse generators and clock recovery circuits, ultrafast A/D-converters, and in multi-photon microscopy.

These are just a few examples. Once ASPICs get to be really cheap, they will offer ample opportunity for small and large companies to improve their competitiveness by applying them in their products.

Applications

The Ecosystem for Photonic Chips

Successful introduction of a novel technology requires a close interaction between users and providers of the novel technology. Figure 3 depicts the main players in the eco-system.

At the heart are the generic foundries that provide cost-effective access to their high-performance technology. But the largest group, both in number and market volume, is formed by companies using Photonic ICs in improved or novel products, for a variety of applications in telecom, datacom, sensing, security, medical diagnostics and metrology. Many of them are SMEs that do not have the expertise to design a chip themselves. A third key actor is, therefore, the group of PIC designers that forms the bridge between the users and the foundries by translating the functional requirements of the users into a PIC design that can be processed in the foundry. This is quite similar to the model in microelectronics where design houses play an important role in making microelectronic technology accessible to small companies. For the designers, to reduce their design time and the number of design cycles required, it is important to have dedicated design software with an accurate description of the foundry technology and accurate component libraries. The fourth key group provides the R&D that drives a dynamics similar to Moore’s law in electronics by developing new generations of foundry technology with ever increasing performance, by developing increasingly powerful design software, component and sub-circuit libraries, and by developing advanced Application Specific Photonic ICs (ASPICs) for novel or improved user applications.

For an effective development of the ecosystem a coordinated approach (a broker) is necessary, which covers the following tasks:

- Combining designs from different users on Multi-Project Wafer (MPW) runs. In this way the costs of R&D runs can be shared by many users, which leads to a dramatic reduction of the entry costs.
- Organising proper design documentation and training for the available foundry processes.
- Informing potential users and discussing the opportunities that the novel technology brings for their product portfolio. Bringing them into contact with designers with expertise in their field.
- Developing and yearly updating a roadmap for the field.
- Stimulating cooperative research projects for realising the roadmap.
- Representing the JePPIX partners in national and European bodies.

In the FP6 Network of Excellence ePIXnet, three platforms have been created for the most important generic technologies that, together, cover a major part of the applications market: JePPIX for InP-based monolithic integration technology, ePIXfab for silicon photonics technology, and TriPleX for low-loss high-Q dielectric waveguide technology. ePIXfab and JePPIX have taken up the brokering role in their fields, but without adequate funding for JePPIX. For TriPleX there is no broker yet, but there are good opportunities for combining this with JePPIX.

1 www.jeppix.eu
2 www.epixfab.eu
3 www.lionixbv.nl/integratedoptics/triplex

Figure 2 Widely tunable laser for application in optical coherence tomography.

Figure 3 The main actors and their relationship in the generic foundry ecosystem.
In 2009 and 2010 the JePPIX consortium started research on a second generation (G2), which provides small scale access for research purposes to its foundry platforms. These projects will provide access to 10-20 internal and external designers per year for integrating lasers and optical amplifiers. It is, therefore, the material of choice for photonics, and silicon is the material of choice for electronics. COBRA recently started research on a third generation (G3), which provides the same photonic functionality as G1 and G2 in an InP-based membrane-layer on top of a silicon or CMOS substrate. If successful, it will become a successor of G2, offering efficient integration of photonic and electronic functionality. It is still in an early stage, however. Its commercialisation is not expected before 2020.

The guiding model for the proposed approach is the US MOSIS program\(^1\) that made silicon VLSI technology accessible to a broad community in the past decades (more than 50,000 designs). In a first phase it provided free access for universities to a number of silicon foundry processes. This provided the program with a huge leverage; it attracted a large number of PhD students and other designers whose salaries were paid from other sources. A significant number of these designs have led to very successful products and companies and given a large boost to the development of VLSI technology. The model can be repeated in photonics with modest government investments. Figure 6 illustrates the market roadmap. It can be divided in four phases.

**Phase 3.** Within the JePPIX platform a plan for creating national design centers for interesting and assisting national university users has gained broad support. The plan foresees the setting up of seven JePPIX design support centers, in addition to the Dutch center at COBRA, in the UK, Germany, France, Poland, Sweden, Italy and Spain. Other countries will follow. Figure 6 (R&D prototypes) shows a conservative estimate of the number of designs that these national centers can generate by mobilizing and assisting interested designers from universities and companies. In take off, Phase 3 will need some modest Support-Action like funding.

**Phase 4** is the production phase that will follow from successful business cases generated by phase 3. The market that will be generated in this phase is estimated to take off after 2015 and to exceed 1 B€ before 2020. The underlying assumptions are summarized in the Appendix.

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\(^{1}\) See footnote on page 4

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**Technology Roadmap**

As a result of significant investments in developing a foundry technology infrastructure (over 50 ME in European and national projects) Europe is making substantial progress towards establishing this new way of working. Figure 4 shows the roadmap for InP-based technology.

**Market Roadmap**

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**Phase 1.** In 2007 the COBRA institute of TU/e started providing small scale access for research purposes to its generic integration technology in the framework of the JePPIX platform (1 MPW-run with ~5 designs per year).

**Phase 2.** In 2009 and 2010 the JePPIX consortium started the EuroPIC and the PARADIGM projects for exploring the feasibility of transferring the generic approach from a university environment to industrial foundry platforms. These projects will provide access to 10-20 internal and external designers per year in the period from 2011-2014, most of them from universities and SMEs.

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**Figure 4** Roadmap for three generations of InP-based generic foundry technology.

Since 2007 COBRA has provided small scale access to a first generation (G1) research platform. Process capabilities have been gradually improved and presently support design of ASPIC integrating lasers, optical amplifiers, modulators and detectors with 10 Gb/s speed, and a variety of passive optical components.

In 2009 the EuroPIC project began with the mission of transferring the foundry model from a university environment to industrial and semi-industrial platforms (wafer fabs of Oclaro and FhG-HHI) and starting development of software design kits and standardized packaging solutions. The project has recently delivered its first chips from foundry trials relying on generic building block technology and is preparing a second full foundry run with access for a few external users. After the end of the project in 2012 R&D will be started to prepare commercialisation. Full commercial operation can start after 2014, if the foundry model proves sufficiently viable at that time. Until that time, access to external users will be provided on a limited scale on a best effort basis.

In 2010 the PARADIGM project has started with development of a second technology generation (G2) with improved capabilities and performance: capability of providing both transmitter and receiver functions with operation up to 40 Gb/s, availability of superior lasers and amplifiers, wider choice of emission and detection wavelengths and other advanced features. The project will be competitive with advanced application-specific technology, but at a much lower cost. Further the project envisages development of low-cost generic packages and sophisticated software design kits with powerful component and sub-circuit libraries. The processes should be demonstrated before the end of 2014. During the project small scale access will be provided for selected external users. Assuming a viable business case, full commercial operation could start between 2016 and 2017, with earlier access for R&D purposes.

The next step will be the integration of photonics and electronics. Today the dominant approach for wafer-scale integration uses silicon for both the photonic and the electronic functionality.

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**Figure 5** Complexity development of silicon and InP-based ICs.

As seen from figure 5, InP is leading silicon photonics in circuit complexity, because of its superior properties for integrating lasers and optical amplifiers. It is, therefore, the material of choice for photonics, and silicon is the material of choice for electronics. COBRA recently started research on a third generation (G3), which provides the same photonic functionality as G1 and G2 in an InP-based membrane-layer on top of a silicon or CMOS substrate. If successful, it will become a successor of G2, offering efficient integration of photonic and electronic functionality. It is still in an early stage, however. Its commercialization is not expected before 2020.
**Chip Cost Roadmap**

**Chip cost.** Todays InP-technology is based on 3” wafers. A batch of 4 wafers has a usable chip area > 10,000 mm². If we assume that the costs of such a batch are in the order of 100 k€, as an example for a process with moderate complexity, the chip cost will be in the order of 10 €/mm². If the wafer volumes for foundry technology grow the costs will rapidly sink below 5 €/mm². Chip cost for small ASPICs can thus get below 10 € even for small volumes. With the assumptions described above an ASPIC with more than 40 components on 6x6 mm², as the one shown in figure 1, will cost 350 €. This is a very small fraction of the cost of the individual discrete components (1 AWG demultiplexer, 20 SOAs and 20 phase modulators, estimated cost today 25-50 k€). In the longer term (>10 yrs) further reduction below 1 €/mm² may be expected by improving the fabrication process (yield) and increasing wafer and batch size. Yield of generic processes will compare favourably with application-specific ones because R&D investments can be focused on standardized processes only.

**Cost of a design run.** For designing a complex ASPIC to a given specification a few design runs may be required. By combining a number of designs on a so-called Multi-Project Wafer run the costs of a full run can be shared by several users and with the assumptions described above each user will pay around 200 €/mm² for a chip set containing some 20 chips, which is usually sufficient for test purposes. Even for a design cycle of a few runs the chip costs remain affordable for many users. This compares very favourably with the development of an application specific process for a chip, which costs a few hundred thousand up to a few million Euro, dependent on the complexity of the process and the chip.

**Cost of design.** In the generic foundry approach the costs of developing a chip are no longer dominated by the chip cost but by the salary costs of the designer who may need many months of work to come to a good design. These costs will be strongly reduced, by the development of dedicated design kits with accurate libraries which allow for rapid and accurate chip design. As a result we expect that in the coming 5 years the design time will be reduced by a factor between two and five.

**Packaging cost.** Another important cost factor is the packaging of the chip. Even now the packaging costs are usually larger than the chip costs. This comparison will become worse when the chips become much cheaper. The PARADIGM consortium is, therefore, developing a standardized generic package for a broad class of different chips with standardized positions of the optical and electrical input and output ports. Costs of the packaging are expected to reduce to a few hundred Euro for small volumes and a few tens of Euros for very large volumes.

**InP and silicon photonics.** Due to the reduction of chip costs in a generic foundry model other costs, like the costs of design and packaging, will dominate the application costs. Because they are similar for InP and silicon photonics technology the cost per square mm of a technology is, up to a certain extent, less important than the functionality that it offers on that square mm. We see, therefore, excellent opportunities for InP for more complex circuitry, whereas silicon may prove more competitive for less complex, very high-volume PICs. Hybrid combination of both technologies will prove advantageous for both and is a good topic for a joint R&D effort. In the longer term we expect a merger of InP and silicon technology, as depicted in figure 4.

**R&D Roadmap**

For a development in Photonics with a steady increase in performance and capability at constant or even decreasing cost (similar to Moore’s law in microelectronics) a continuing R&D investment program is necessary in the three fields indicated in figure 3. They will be discussed subsequently.

**Software and library R&D** is important for shortening the design cycle by developing accurate and comprehensive simulation of the ASPIC performance, so that only a few or even a single fabrication run is sufficient to arrive at the required performance. R&D should be focused both on increasing the simulation and mask-layout generation capabilities of the software, and on development of accurate component and sub-circuit libraries. The former will be the main responsibility of the software companies, the latter offers excellent opportunities for university-based research, in close cooperation with the foundries.

**ASPIC-design.** A third field of research is the development of ASPICs for specific user applications. Here universities will play an important role. In the coming years development of advanced ASPICs for specific applications will be a challenging task for PhD students, and a lot of the research that is presently being done on development of discrete photonic circuits and sub-systems will shift to development of ASPICs. This means that part of the funds available for component and system research may be directed towards development of generic ASPICs, which will provide the foundry approach with a large leverage.

In the longer term we expect that ASPIC design will shift increasingly to companies and design houses, with universities remaining active on ASPIC development for advanced applications.
Establishing an investor board with both national and European level.

National and regional funds should stimulate the use of ASPICs by local companies.

European funds should stimulate investments in foundry technology and infrastructure development for which the costs are too high to be carried by a single country, and the risks are too high to be carried by a single company.

Such funding will be crucial for bridging the valley of death between the R&D prototype phase and the production phase as shown in figure 6.

Project funding should address research in the three fields mentioned in the R&D roadmap:

- Process technology, testing and packaging R&D
- Software and library R&D
- ASPIC-design

Process technology and packaging R&D is significantly more expensive than software and ASPIC development, and less suited for national funding, they should preferably be supported by creation of a European investment fund.

Selection of projects should preferably be done by a selection committee with a mix of national and European reviewers. The JePPIX platform can provide guidelines and support for evaluation of national and regional projects in order to achieve a coherent European approach. For projects with public co-funding special attention should be paid to models that can, on a longer term, provide a return on investments from successful projects, which can be re-invested in novel R&D. In this way the dependence on direct government funding will be reduced in the longer term.

Successful development of the foundry model requires an intensive cooperation between many partners in the ecosystem. Good coordination is of key importance for the success of the novel approach. As the JePPIX platform is presently recognized as a coordinating body by all key players in the InP-based foundry approach it is the instrument par excellence for coordinating the future development.

At present JePPIX is an informal organization, supported by TU/e and a few other partners on a voluntary basis. It organizes yearly training in PIC-design, including some fabrication technology background, and it organizes MPW-runs on the COBRA research process, including designer support and assembly of the user designs in a single mask set. Another important role is the coordination of existing and new R&D projects for further development of the foundry infrastructure. Finally, it is building a member group of users, from both universities and companies, that are interested in the use of ASPICs. At present this group numbers more than 80 users.

JePPIX is one of the three integration technology platforms that were created and funded by the ePIXnet Network of Excellence. After completion of ePIXnet, funding of the silicon photonics platform ePIXtab was continued, but funding of the InP-based platform JePPIX and the dielectric waveguide platform TriPleX was stopped. Despite lack of funding the JePPIX platform has been extremely successful in bringing the InP-community together in a coherent effort for building a generic foundry technology infrastructure. For bridging the valley of death a similar funding as provided for the silicon photonics platform is highly desirable for enabling the JePPIX and the TriPleX platforms to take up the rapidly growing burden of user support.

Step 1: Appointment of a full-time coordinator with the tasks as described under “Funding Roadmap” (page 12)

1 UK (University of Cambridge), Germany (Karsluhe Institute of Technology), Sweden (KTH-Stockholm), Spain (UPV), Italy (Politecnico di Milano), Poland (Warsaw University of Technology). Discussions in other countries are in progress.
SWOT Analysis

Strengths:
- Strong existing knowledge base
- ASPIC Technology capable of meeting user specifications now
- Close, JePPIX-led, cooperation between the main stakeholders
- Clear lead over other (non EU) countries

Opportunities:
- Build dominant ASPIC based businesses in Europe
- Create clearly differentiated business chain
- Design
- Fab
- Packaging
- Software tools
- Applications houses
- Achieve, straightforward, low cost access to ASPIC technology for all

Weaknesses:
- Too dependent on university sector
- User base still too small, many companies not aware of opportunities

Threats:
- InP fab operators cannot make necessary scale of investment, slowing progress
- Large strategic foreign government led investments.

Appendix: Market Roadmap Assumptions

The market prediction as shown in figure 6 is based on the assumption that the development of commercial ASPIC applications will take place in two phases.

**In a first phase** it will be university driven, just as in microelectronics in the MOSIS program. In the projects EuroPIC and PARADIGM we see that many universities are interested to gain access to foundry processes. Many of them work in close cooperation with companies and a number of their designs will translate into commercial designs. This first phase can be launched with modest funding at the university side, because the major cost, salary cost for PhD students, will come from other existing or new projects, which will provide the investments in the foundry infrastructure with a large leverage. Crucial to the success of this first phase is the availability and accessibility of the technological infrastructure, which requires large public-private investments on a European scale.

The second phase will typically start 2-3 years later, after the results of the first university designs become clear and a number of these design appear to be sufficiently promising for transfer to a company (either existing or a startup). As the companies will get little return on their investments during the first years, public co-funding may prove vital for getting the wheel turning. These investments can be done on a national or regional scale.

The quantitative assumptions underlying figure 6 are as follows.

At present JePPIX users run 5-10 designs per year on the COBRA process (the blue bars in figure 6 for 2009-2012). In the EuroPIC and the PARADIGM process 10-20 users (both internal and external) are designing in the experimental processes of Oclaro and Fraunhofer-HHI (the green bars). During and after EuroPIC and PARADIGM the design effort should be taken over and expanded by the national design support centers mentioned in the organization roadmap. These national centers will contribute an increasing number of ASPIC designs as indicated by the blue bars. Designs will come from both universities and companies, universities will play an important role in transferring this technology to companies.

It is assumed that 20% of the university designs will lead to a commercial design after 2 years (i.e. a design which a company will develop further into a product). Further it is assumed that in 2014 the first commercial ASPICs will go into production. Further we assume that in the first five years the number of ASPICs which reach the production stage will double each year, which is realistic with an active platform dissemination policy. Further it is assumed that from the number of ASPICs in production in one year, 80% will still be exploited in the next year.

The data mentioned above refers to numbers of ASPICs. For translation into a market figure we have assumed that 50% of the commercially successful designs (which is with the present assumptions only 10% of all R&D prototypes) generate a 10 M€/yr business after 2 years, while 20% generates a 100 M€/yr business after 3 years and 5% a 500 M€ business after 4 years.

These assumptions lead to the prediction shown in figure 6.