Tipps
BACK-END Foundry

Stanadrd Generic Test Package G5

Design Rules per October 2018

Receiver
Public

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G5-rev1_0-design rules.docx

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To realize the transfer of ASPIC chip design to commercial product, packaging of chip is crucial step and a great deal of efforts can be saved by taking packaging into account during chip design phase.

Designing customized package for test chip or prototype might be too costly and time consuming. Generic Test Package from Technobis is designed so as to fit a wide group of ASPIC chips into it so as to facilitate the purposes of test chip evaluation or demonstration of idea, resulting in shorter time-to-market.

Generic Test Package is a standard product and ASPIC chip has to be designed by following some general design rules so that the chip can fit easily. This document describes the design rules for the Generic Package.

In standard Generic Test Package, the followings are included:

1. Package Housing;
2. Up to 3 PCBs and Wirebonding from ASPIC to PCBs;
3. Thermal Control Components;
4. Fiber and Fiber Alignment;
5. Assembling.

On the last page of this document there is a checklist of design rules and users, especially chip designers, can quickly check whether chip design matches with design rules or not.

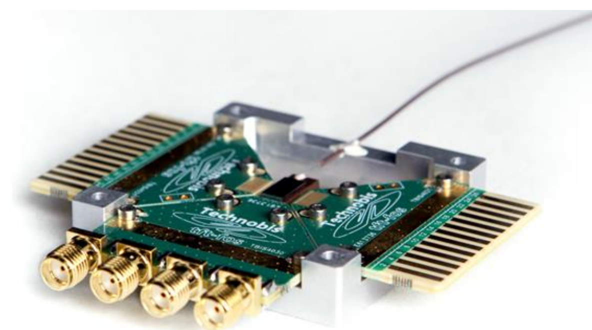

Figure 1. Generic Test Package G5

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Revision

Revision	Date	Changes
1.0	31-Oct-18	Final Version

1 Scope

1.1 Identification

This document describes the design rules for Generic Test Package G5 as shown left. This Generic Test Package is specially developed for prototyping and allows placement of three PCB boards and an ASPIC within a range of dimensions. The design rules are made available through the PhoeniX design kit as well.

Figure 2. Generic Test Package Examples

1.2 System Overview

The Generic Test Package is intended for evaluation of the functionality and performance of new prototype based Application Specific Photonics Integrated Circuits (ASPICs) and can act as a starting point of the development of a dedicated package including front-end electronics.

1.3 Document Overview

This document specifies the general design rules of certain aspects of ASPICs so that the ASPICs coming out from different foundries can easily fit into our G5 package. The design rules concern:

- ASPIC Floorplan;
- Optical I/Os;
- Electrical I/Os.

2 ASPIC Floorplan

2.1 ASPIC dimensions

G5 package can accommodate ASPICs of different sizes. Minimal dimensions are 3.5mm x 2mm and maximum are 6mm x 6mm. Smaller or bigger ASPICs are most of the time not a problem and please consult **Tipps** on advices over non-compliance in dimensions.

2.2 Optical I/O and bondpads locations

In order to fit in the G5 package the ASPIC should

have the layout as depicted on the right.

With the ASPIC orientated such that optical I/O is on **North** side, the other three sides are reserved for electrical bondpads. The bondpads should be arranged in the following order:

1. **East**: PCB board on East side is imperative (in case there are TEC or/and bondpads on ASPIC);
2. **West;**
3. **South.**

IMPORTANT:

1. All optical I/Os and electrical bondpads should align to ASPIC edges;
2. There should be no edge with both optical I/Os and electrical bondpads.

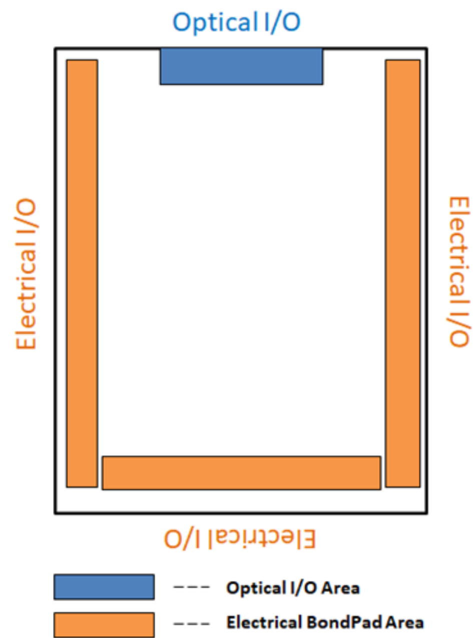

Figure 3. ASPIC standard layout

3 Optical I/O

3.1 Active Fiber Alignment

Active alignment will be done through maximizing signal from probed on-chip photodiode or on-chip laser output. Operation instructions (e.g. which photodiode should be probed) will have to be supplied to **Tipps.** Different types of fibers are available and the arrangements of optical I/O should follow the specifications stated in Section 3.2 and Section 3.3.

3.2 Single Fiber

For signal optical I/O, the I/O waveguide can be straight or at an angle, positioned at:

- **Straight I/O**: **Centered** along chip facet (Figure 4a)
- **Angled I/O**: **1mm off-center** along chip facet. The direction of offset depends on the angle, as in Figure 4b. Note that if the width of ASPIC is <4mm, I/O should be centered even it is angled.
- **Vertical Grating Coupler (VGC)**: **Centered** along chip facet and **1mm from edge** for gluing (Figure 4c).

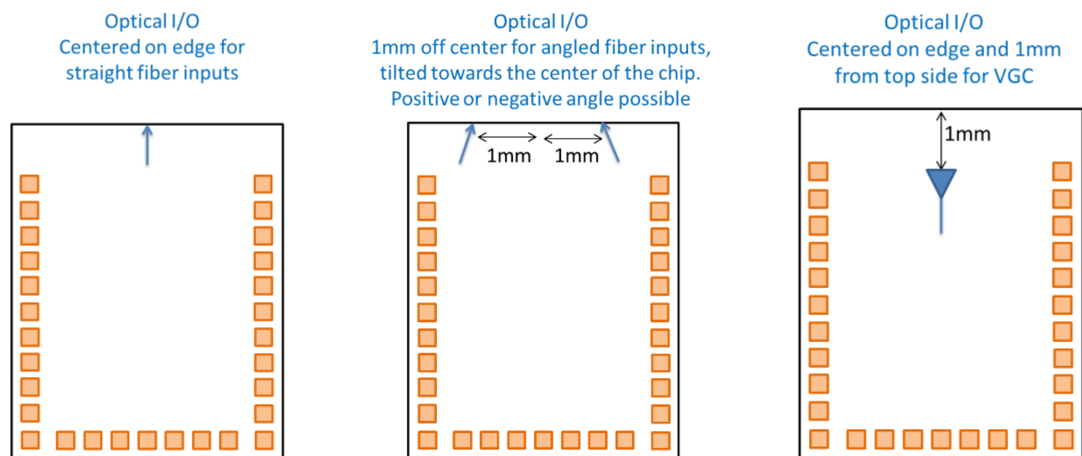

Figure 4. Optical I/O arrangement for single fiber: (a) Straight (Left); (b) Angled (Mid); (c) VGC(Right)

Possible fiber types	Description
Lensed SMF	For optical I/O waveguides with 3µm Spot Size Converter
Cleaved SMF	For optical I/O waveguides with 10 µm spot size converters
Lensed PMF	For optical I/O waveguides with 3µm Spot Size Converter
Cleaved PMF	For optical I/O waveguides with 10 µm spot size converters
Angled cleaved PMF	For Grating coupler designed to match with 10µm core fibers
AR-coated fiber	Specified for 1550nm CWL

Platform	Possible waveguides
InP	Edge coupled waveguides - Straight 10 µm spotsize converter - Angled 10 µm spotsize converter - Straight waveguides with 3 µm spotsize converter - Angled waveguides with 3 µm spotsize converter
SOI	Vertical Grating Couplers (VGC) - 40° cleaved fiber

3.3 Fibers on opposite sides

In case more than one fiber is needed, there can be a second optical I/O along the South side. The configuration is depicted in Figure 5.

Note: There should not be electrical bondpads on the South side when there is the second optical I/O.

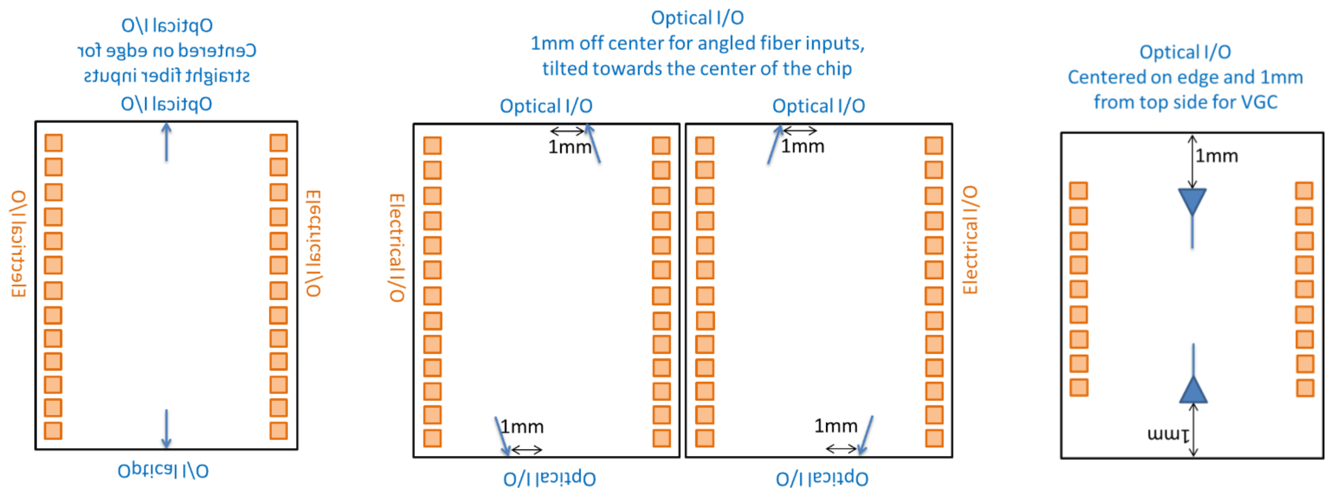

Figure 5. Optical I/O arrangement for Fibers on opposite sides: (a) Straight (Left); (b) Angled (Mid); (c) VGC(Right)

4 Electrical I/O

4.1 General

In the G5 Generic Test Package, **up to 3 PCB boards (DC/RF)** can be around ASPIC (Figure 6).

With the ASPIC orientated such that optical I/O is on **North** side, the PCB board on **East** is imperative. TEC and thermistor will be connected (using pins 1, 2 and 3, 4 respectively) to this PCB and would be a DC PCB board. PCBs for South and West slots can be DC or RF.

Important: There should be no edge with both DC and RF pads.

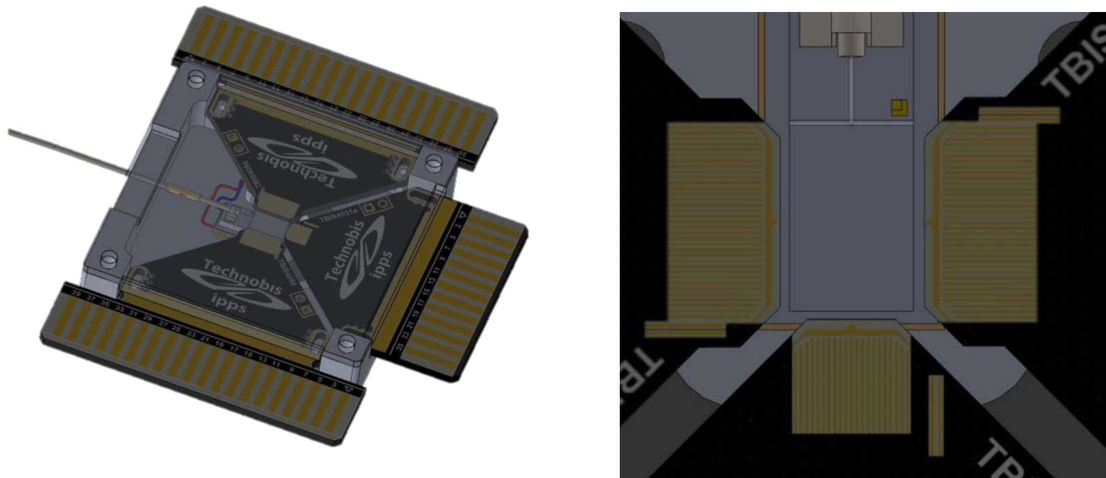

Figure 6. Configuration with 3 PCBs: Two 40-pins DC on left and right to input fiber and one 26-pins DC opposite to fiber

4.2 DC Electrical Connections

Two types of DC boards are possible, a 40-pin and a 26-pin version. Note that some pins are reserved for TEC, thermistor and GND. Thus, the max number of bondpads that can be connected to are **35** and **21** respectively.

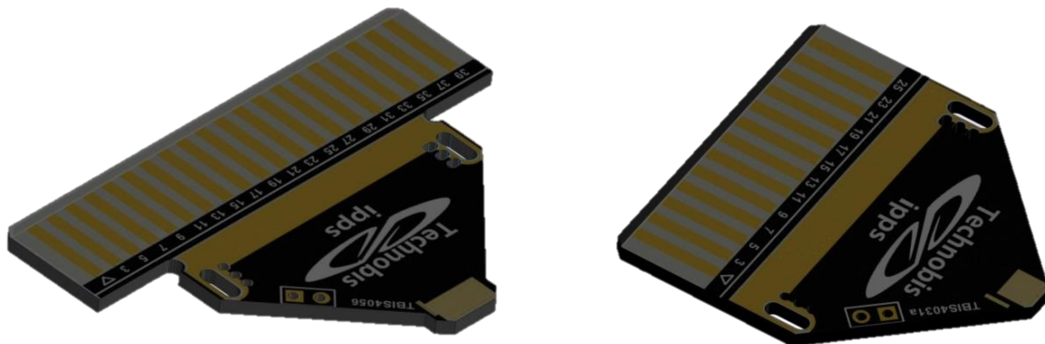

Figure 7. 40-pin PCB (left) and 26-pin PCB (right)

4.2.1 ASPIC Design Rules to use the above DC PCBs

Aspect	Descriptions
Pad Size	100 µm x 100µm
Pitch	180µm
Max pad number	max of 35 bondpads along longer edge and 21 bondpads along shorter edge
Pad location	As closes as possible to the edge (in the order of 100 µm). Arrange the bondpads according to the sequence in Section 2.2.

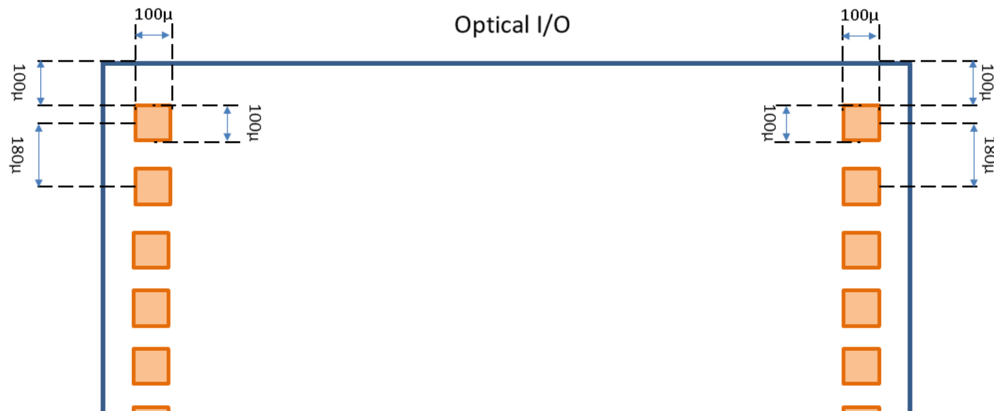

Figure 8. Arrangement of DC bondpads along East and West

4.2.2 Ground Pad(s) on ASPIC

There are 4 grounding options (foundry-dependent, only one of the four is applicable on one chip). Note that in the normal configuration of G5 package, **Ground line is connected to the housing**. If that is not desirable, please arrange Ground pad on chip as one of the signal pad, as in Option 2 below):

1. Common ground through the bottom pad on **East** side: The top bondpad can be an additional ground pad. They are connected to the housing and other PCB's grounds as well (Pin 5 on all DC boards).
2. Ground pad(s) as signal pads: Ground pads will be
3. connected to separate pins and thus not to the standard ground(s) and housing. However, as some signal pins are used for Grounding, the max number of signal pins is reduced.

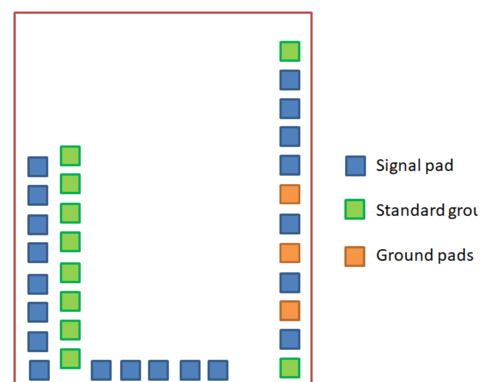

Figure 9. Ground Pad allocation options

4. Staggered: Behind the signal pads. All these grounds will be connected to Ground pad on PCB. The pitch between ground pads is 180µm and the effective pitch between signal and ground pads is 90µm.
5. Ground through bottom of the ASPIC

Note: all PCB boards are grounded to the housing and ASPIC standard ground(s).

4.2.3 Bondpads along East and West edges (bottom pad alignment)

- First pad to be placed should be closest to **South** edge, as close as possible to the edge and corner (typically 100 µm).
- Add pads towards the **North** direction until end of ASPIC.
- See 4.2.2 for the ground pad(s).

4.2.4 PCB on South side (central alignment):

- Start from the center (first pad) and add pads evenly on left and right
- For even number of bondpads, there is one more pad towards West than towards East.
- Place pads as close as possible to the **South** edge (typically 100 µm).
- See 4.2.2 for the ground pad(s).

4.3 RF Electrical Connections

On each RF board, there are 4 single-ended RF connection (GSG), connectable using SMA-connector (*Figure 10*).

Typically, each connection can handle 1GHz signals.

EMI Gaskets will be used to reduce the open spaces between case and lid of the housing.

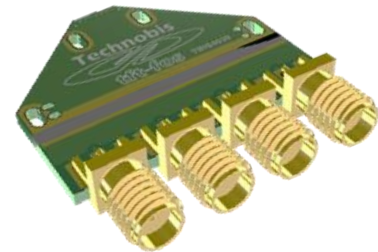

Figure 10. RF Board with 4 SMA connectors

4.3.1 ASPIC Design Rules to use the above RF PCBs

Aspect	Description
Allocation	Along South and/or West sides of ASPICs
Max connections	Up to 4 GSG signals per edge (depending on chip length)
Signal pad pitch	Pitch between signal pads: 1700 µm
Ground pad pitch	Pitch between signal and ground pad: 180 µm
Pad size	100 x100 µm
Pad location	100 µm from chip edge
Signal rate	Typical 1GHz

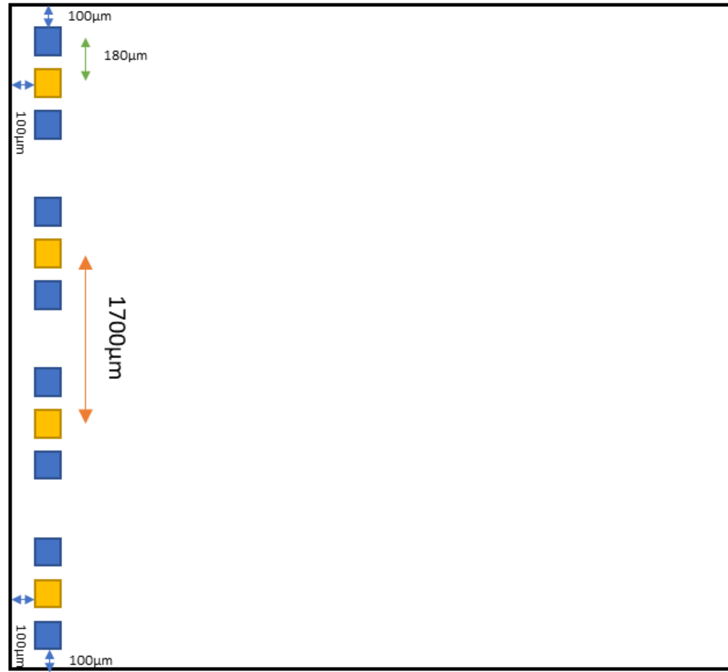

Figure 11. Standard RF (GSG) bondpads arrangement

5 Others

5.1 Thermal control

As all ASPICs are temperature sensitive, most applications require thermal control to maintain stability of PIC temperature. Therefore, the G5 package comes with TEC and thermistor as standard components (*Please inform us if active thermal control is not necessary in advance*).

5.2 Design Kit for Packaging

Currently the design rules are available through the design kit from PhoeniX Software (http://www.phoenixbv.com). The design kit will be regularly updated with new options etc.

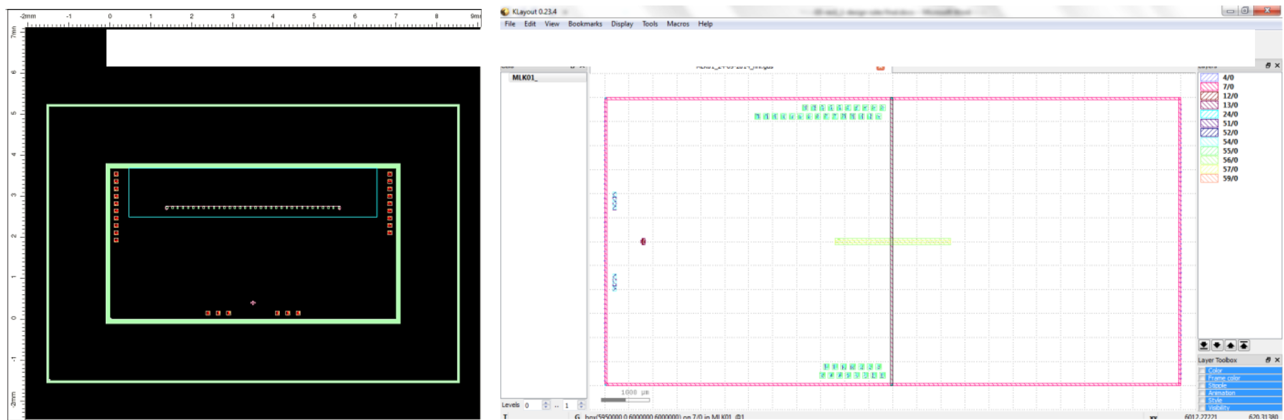

Figure 12. Examples of PDK in Phoenix Software

5.3 Quotation

Contact **Tipps** for final check and quotation.

5.4 Lead time for standard layout

Typically, 4-6 weeks after receiving all parts and paperwork. Additional time might be required for getting parts. Thus, please notify us in time.

5.5 Customized packaging

For production packages we also provide customized package designs, which can include front-end electronics and can be designed for certifications (Medical, Flight approved, Space, etc).

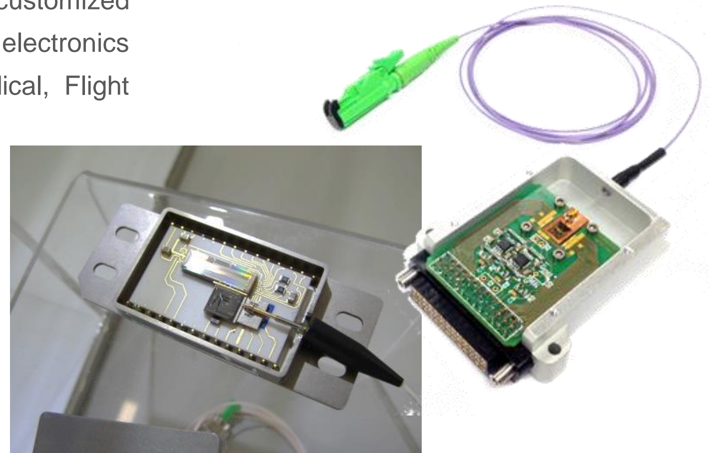

Figure 13. Examples of Customized Packages

5.6 Contact details

Tipps Back-End Foundry,
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info@technobis.com

6 Checklist on ASPIC Design Rules

	ASPIC Design Consideration	Requirement	Compliance
General Layout	ASPIC dimensions	Min: 3.5mm x 2mm Max: 6mm x 6mm	☐
	Chip floorplan	According to Section 2.2	☐
	No edge with both Optical I/O and electrical pads		☐
	No edge with both DC and RF pads		☐
Optical I/O	Location (Only one of the following options)		
	• Straight edge coupling	Center of North side*	☐
	• Straight edge coupling with fibers on opposite sides	Center of North and South sides	☐
	• Angled edge coupling	North edge < 4mm: Center; North edge => 4mm: 1mm off-center[1]	☐
	• Angled edge coupling with fibers on opposite sides	North and South edges < 4mm: Center; North and South edges => 4mm: 1mm off-center[1]	☐
	• Grating Coupler (single I/O)	Center of North side*; 1mm away from edge	☐
	• Grating Coupler (single I/O on opposite sides)	Center of North and South sides*; 1mm away from edge	☐
	Fiber Type (Only one of the following three options)		
	• To use cleaved fiber	10µm SSC on waveguide[2]	☐
	• To use lensed fiber	3µm SSC on waveguide[2]	☐
	• To use Grating Coupler (single I/O)[3]	No specific requirements	☐
Electrical I/O	Allocation of bondpads on chip*	1st: East[4]; 2nd: West; 3rd: South[5]	☐
	First bondpad along East and West edges*	100µm from South edge[6]	☐
	First bondpad along South edge*	At the center of edge; 100µm from the edge[6]	☐
	For DC Bondpads on Chip		
	• Bondpad dimensions	100µm x 100µm	☐
	• Pitch	180µm	☐
	• Ground	Follow specifications in Section 4.2.2	☐
	• Max number of bondpads along a chip edge	35 along long edge and 21 along short edge (excluding ground pads in both cases)	☐
	For RF Bondpads on Chip		
	• Type of connection	GSG	☐
	• Bondpad dimensions	100µm x 100µm[6]	☐
	• Pitch between signal and ground pads	180µm	☐
	• Pitch between neighbouring signal pads	1700µm	☐
	• Max number of bondpads along a chip edge	4	☐
	• Signal rate	Typical 1GHz	☐

*: Note that optical I/O edge is taken as **North** side, refer to *Figure 3* (For Fibers on opposite sides, please inform us in advance)
[1]: Check *Figure 4(b) or 5(b)*
[2]: Specify SMF/PMF
[3]: Only fiber cleaved to 40° is available
[4]: PCB on East side is always used and is always DC connections
[5]: No bondpads on South in case of fibers on opposite sidees
[6]: Check with foundry to see if coating might spread more than that. If yes, please notify us in advance and it can be more than 100µm