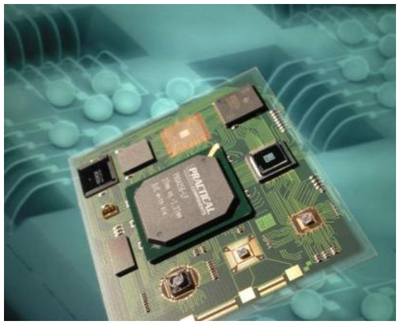
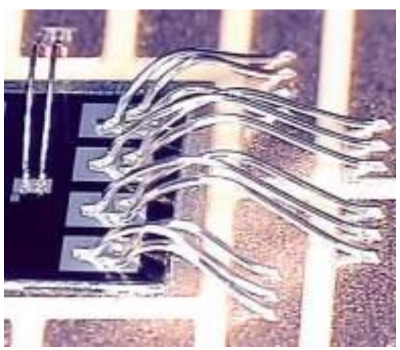
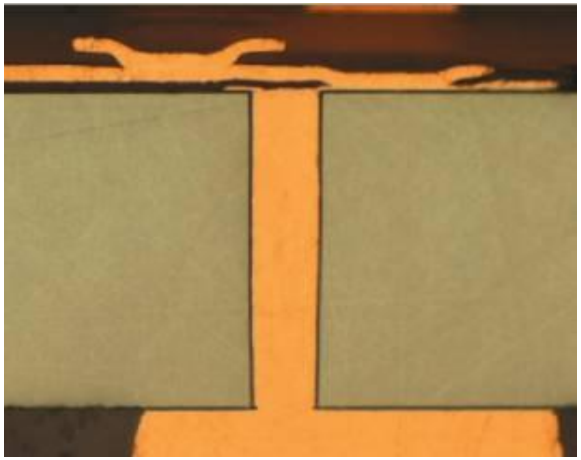




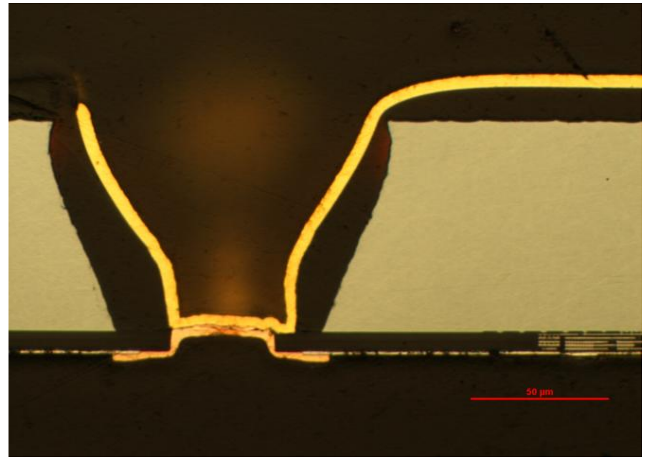
Fraunhofer IZM

Hermann Oppermann

3D Integration Technology



Straight sidewall TSV
for high density through via interconnects
→ Interposer applications



Tapered sidewall TSV
for moderate density through via interconnects
→ Low IO ASIC and sensors

➢ Via last technology after wafer BEOL finish

Dept. System Integration & Interconnection Technologies
Group: Interconnect Metallurgy & Processes
Hermann.Oppermann@izm.fraunhofer.de

3D Integration Technology

Key Technology: Through Silicon Via (TSV) Formation

- Deep Via High Aspect Ratio Etching

  (Ø 3…80µm, AR 1:5…1:10…)

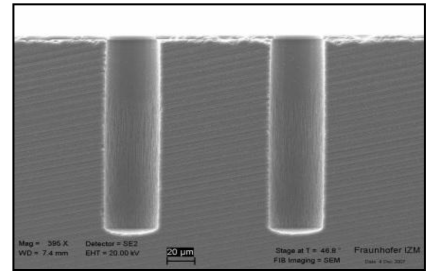
- Side Wall Insulation

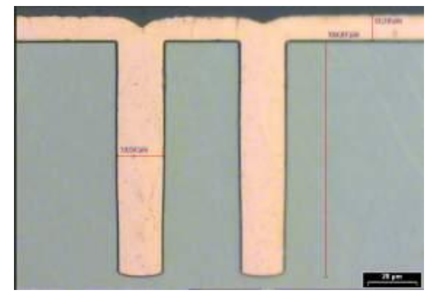
- Deposition of Seed- and Barrier Layers

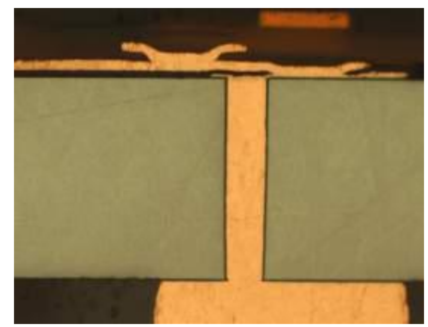
- Via Filling by Cu-Electroplating

  (others: CVD-W, poly-Si)

- Backside thinning and via opening





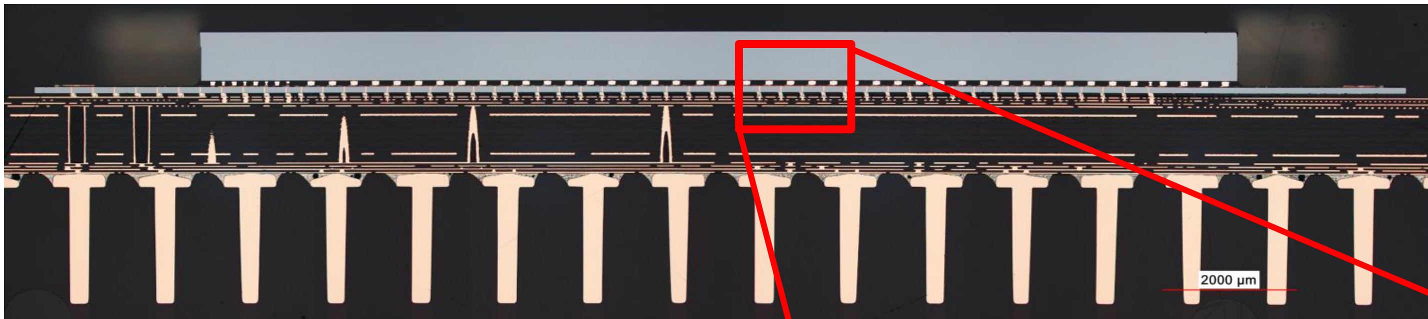


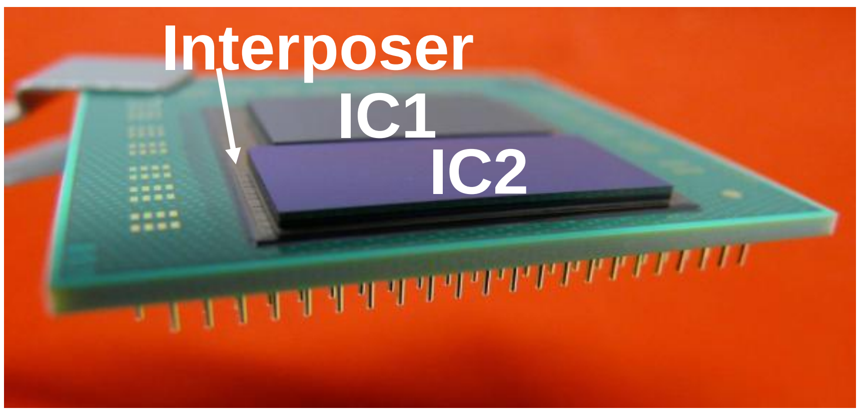
Dept. System Integration & Interconnection Technologies
Group: Interconnect Metallurgy & Processes
Hermann.Oppermann@izm.fraunhofer.de

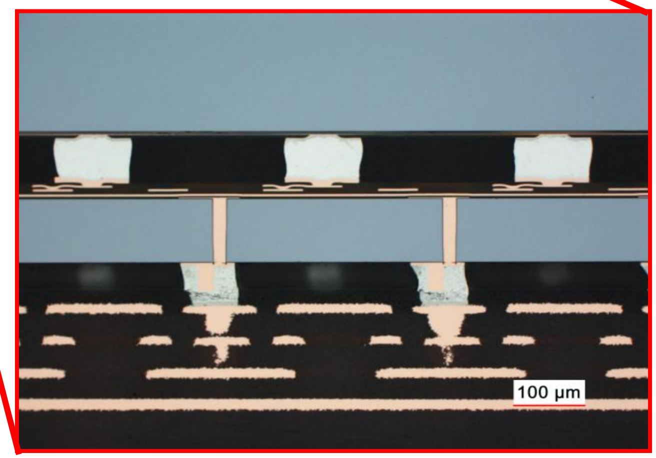
Fraunhofer IZM

3D Integration Technology - Application

3D SIP Module using Silicon Interposer







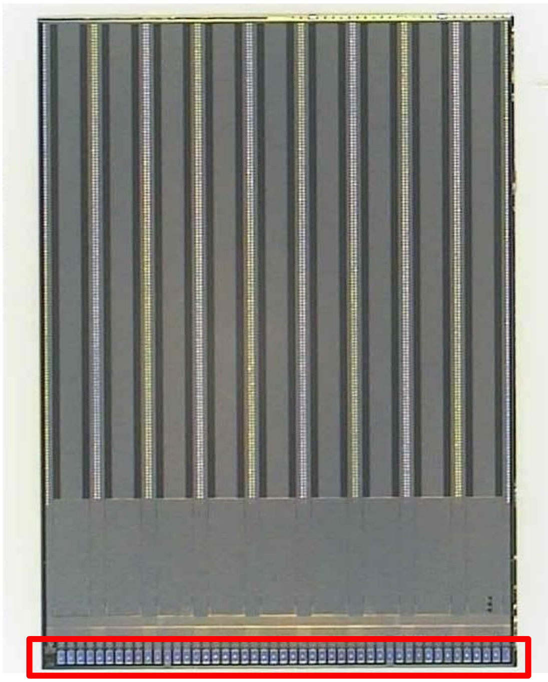
- 42459 TSVs per Device
- More than 200 modules delivered by IZM

Dept. System Integration & Interconnection Technologies
Group: Interconnect Metallurgy & Processes
Hermann.Oppermann@izm.fraunhofer.de

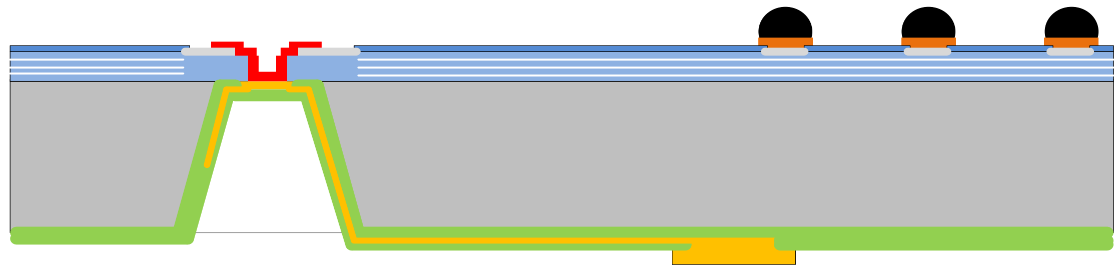
Fraunhofer IZM

3D Integration Technology - Application

Tapered TSVs for 3D ATLAS FE-I3 ROC interconnects



TSV interconnection from backside to peripheral readout chip IOs



Frontside processing:

- Cu pad to bond pad interconnect (red)
- UBM + Bump deposition (black)
- Dicing

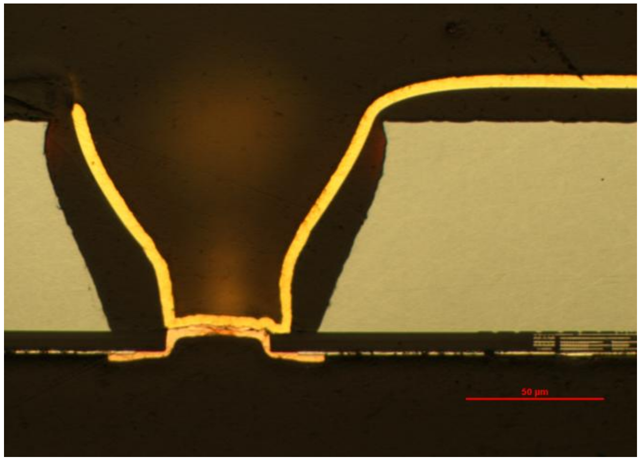
Backside processing:

- Thinning
- Silicon Via etch (white)
- Passivation (green)
- Redistribution Layer (orange)

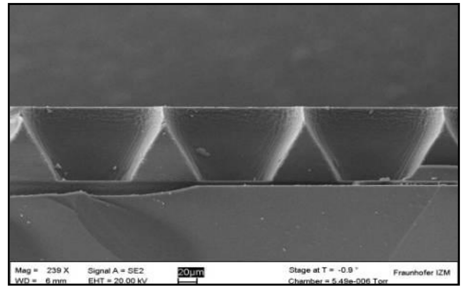
Dept. System Integration & Interconnection Technologies
Group: Interconnect Metallurgy & Processes
Hermann.Oppermann@izm.fraunhofer.de

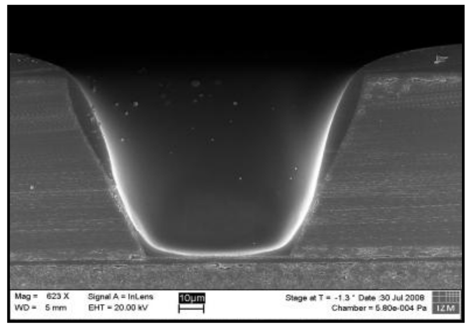
3D Integration Technology

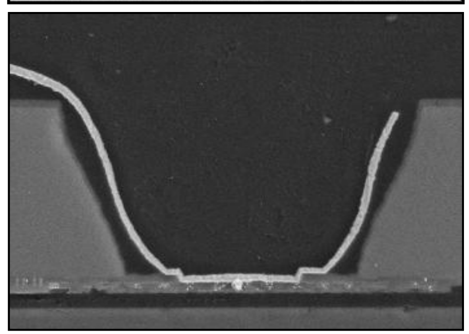
Tapered Sidewall TSV for Low Density IO Interconnects



Tapered sidewall TSV
for moderate density
through silicon via
interconnects
Pitch > 100µm







- Tapered Via Etching
  - side wall angle 74° - 76°
  - bottom Ø 40…50µm
  - top Ø 70…90µm
- Side Wall Insulation (oxide, polymer)
- Deposition of Seed- and Barrier Layers
- Interconnection by Cu-Electroplating

Dept. System Integration & Interconnection Technologies
Group: Interconnect Metallurgy & Processes
Hermann.Oppermann@izm.fraunhofer.de

Fraunhofer
IZM

High Precision Bonding for Optoelectronic Applications (~ 1 µm accuracy in y and z direction)

active alignment = component assembled, and operated during fiber / lens alignment

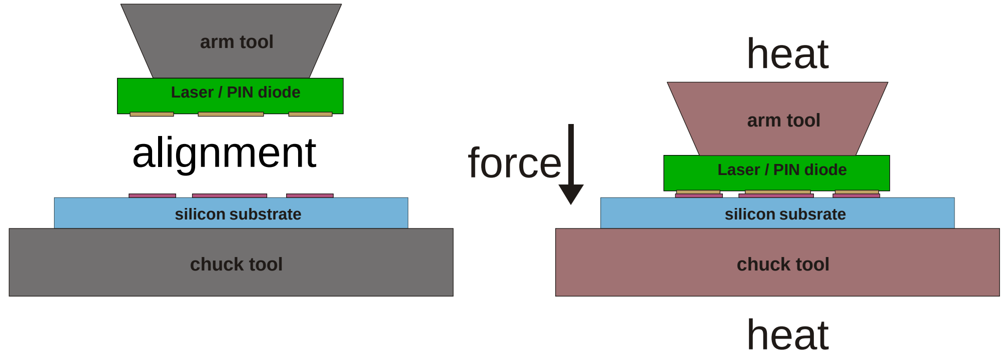
passive alignment = component assembled using an accurate vision system

self-alignment = component placed alignment by surface tension during reflow soldering

Dept. System Integration & Interconnection Technologies
Group: Interconnect Metallurgy & Processes
Hermann.Oppermann@izm.fraunhofer.de

Passive Alignment (precise vision system)

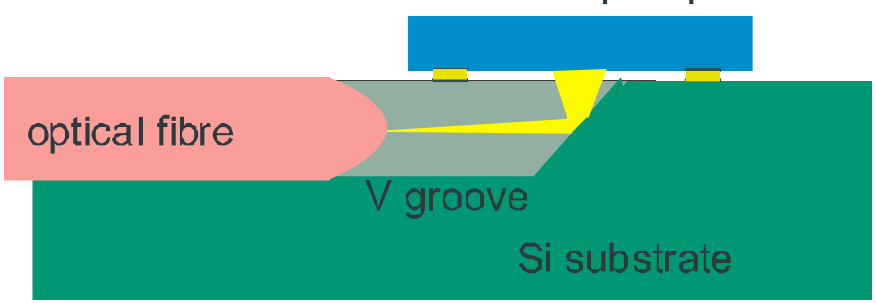
... high precision
thermode bonder:
e.g. SET bonder:
post bond accuracy
$\Delta x, \Delta y, \Delta z < 1\ \mu m$

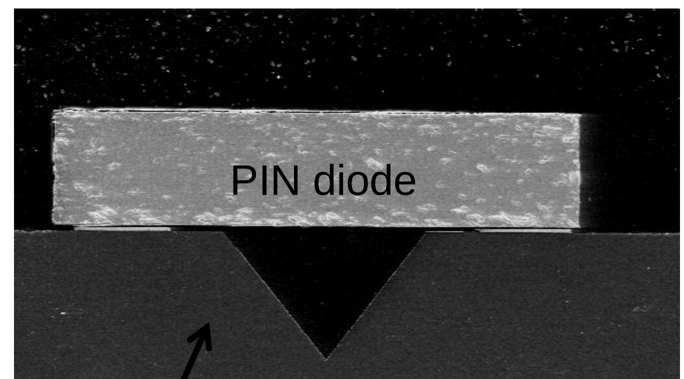


characteristic:

- Au bumps (sometimes AuSn solder)
- highly flexible
- requires precise features for pattern recognition
- long time for pattern recognition and alignment
- long bonding cycle

InP flip chip PIN diode



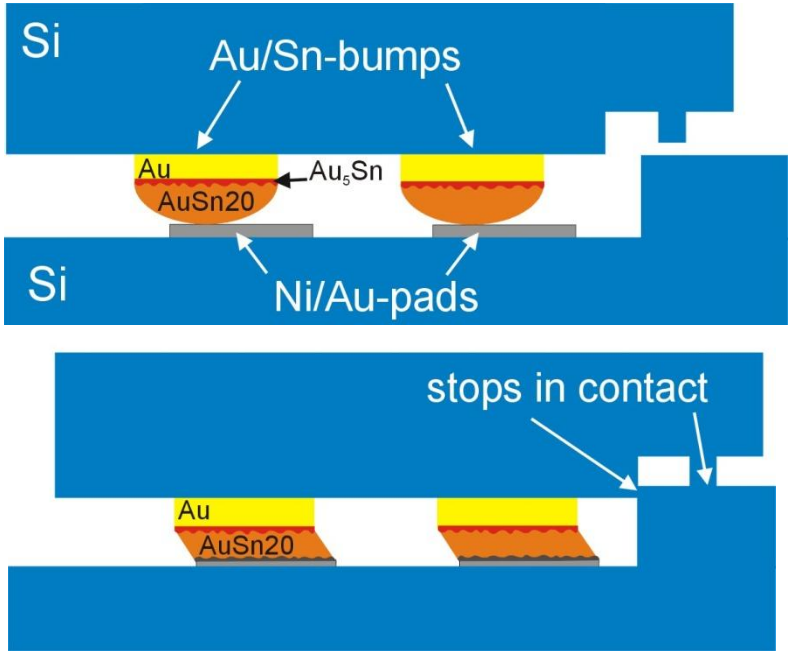


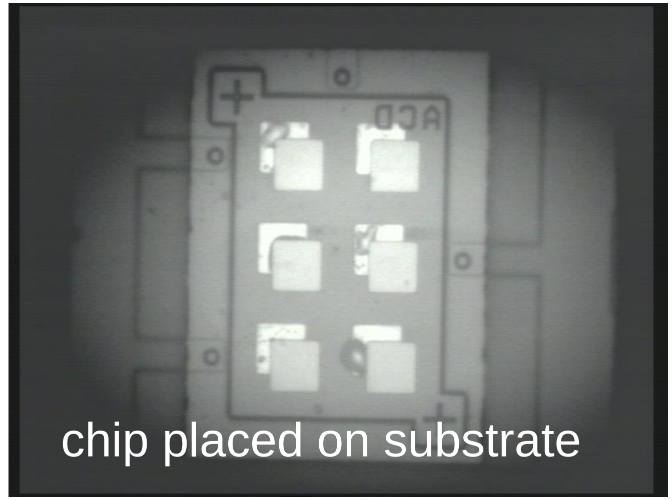
Optical Si bench with mirror and V-groove for fiber clamping

Dept. System Integration & Interconnection Technologies
Group: Interconnect Metallurgy & Processes
Hermann.Oppermann@izm.fraunhofer.de

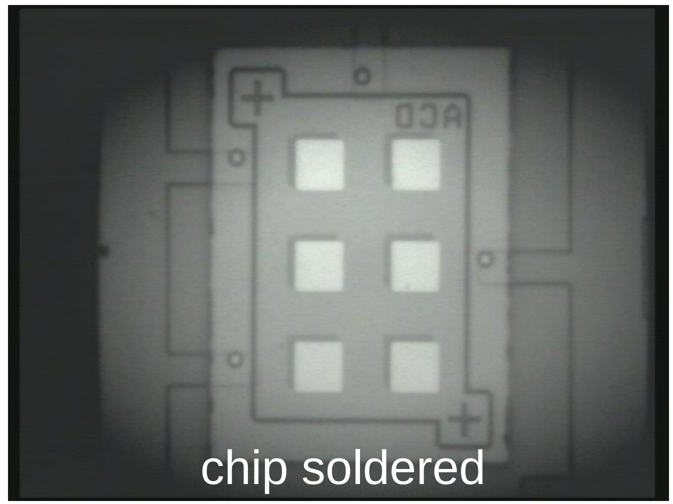
Fraunhofer IZM

Self-Alignment with Mechanical Stops





chip placed on substrate



chip soldered

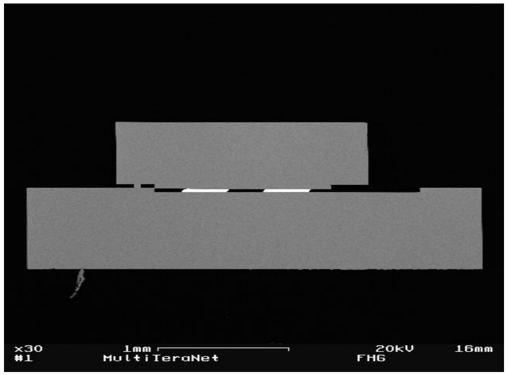
characteristic:

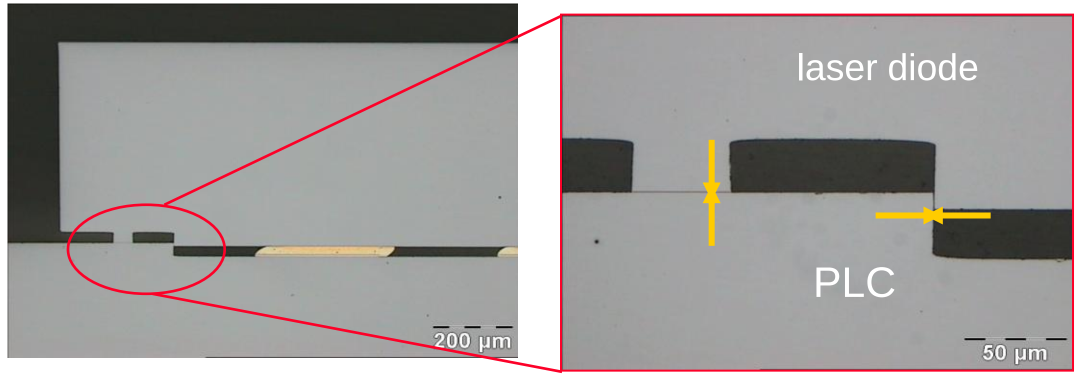
- AuSn bumps (creep resistant, no flux)
- pick & place (low accuracy)
- common reflow of AuSn solder (300°C, few seconds peak)
- self-alignment during soldering
- short bonding cycle

Dept. System Integration & Interconnection Technologies
Group: Interconnect Metallurgy & Processes
Hermann.Oppermann@izm.fraunhofer.de

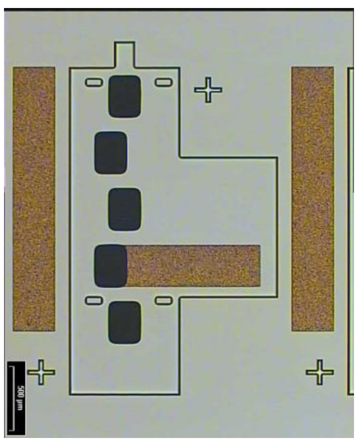
Fraunhofer
IZM

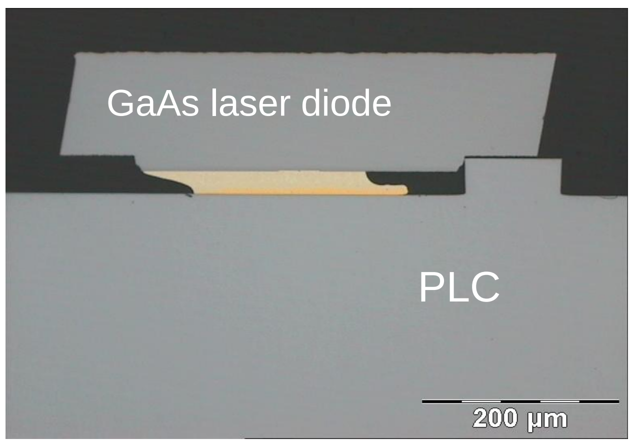
Flip Chip Self-Alignment with mechanical stops





Test vehicle in Silicon with AuSn bumps





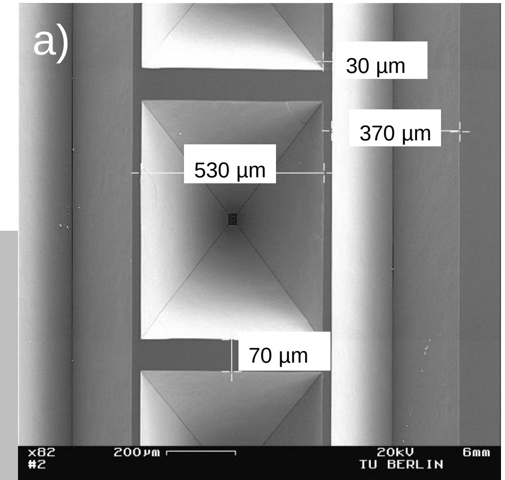
Pump Combiner
Fiber Amplifier

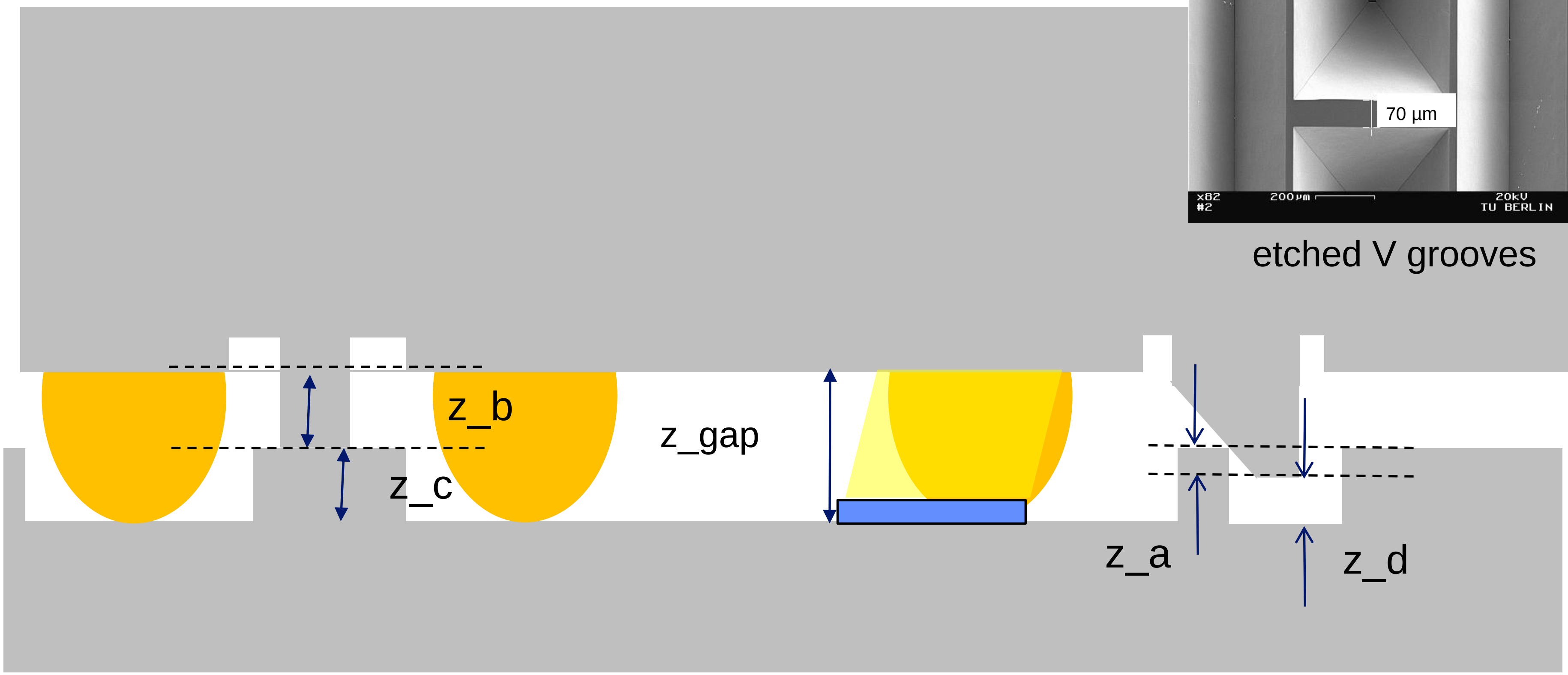
- 4 pump laser
- planar lightguide circuit (PLC)
- AuSn solder bumps
- passive alignment in x-y-z
- 1 µm Post-bond accuracy

Dept. System Integration & Interconnection Technologies
Group: Interconnect Metallurgy & Processes
Hermann.Oppermann@izm.fraunhofer.de

Fraunhofer IZM

Height related Dimension





$z_c = z_{gap} - z_b$ µm

$z_d = z_c - z_a$ µm

Dept. System Integration & Interconnection Technologies
Group: Interconnect Metallurgy & Processes
Hermann.Oppermann@izm.fraunhofer.de