


HELIOS and ePIXfab

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MINATEC CAMPUS



Basic information about HELIOS

- Large-scale integrating project (IP)
- Start date: 1 May 2008
- Duration: 48 months
- Total EC funding: 8.500 M€

Consortium


Industrial end-users

III-V industrials

CMOS foundries and design tools experts

CMOS photonics institutes

Academic labs



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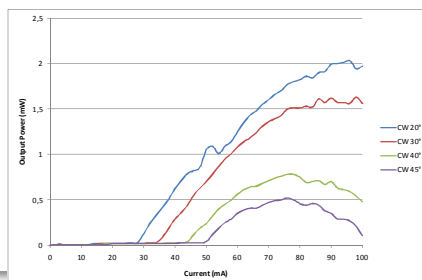
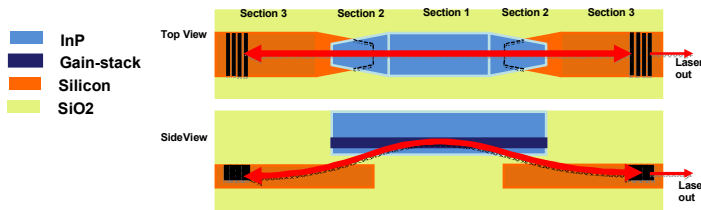
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Objectives

- Build a complete **design and fabrication chain** enabling the integration of a **photonic layer** with a **CMOS circuit**, using **microelectronics fabrication processes**:
 - Development of high performance generic building blocks :
 - **WDM sources by III-V/Si heterogeneous integration**
 - **Fast modulators and detectors**,
 - **Passive circuits and packaging**
 - Building and optimization of the whole “food chain”
 - Investigation of more promising but challenging alternative approaches for the next generation of devices
- It will make accessible integration technologies for a broad circle of users in a foundry-like, fabless way

Main results (1)

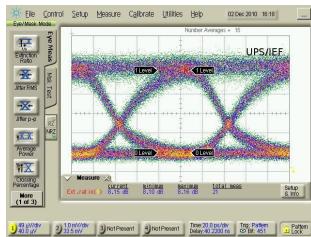
- Design and fabrication of hybrid III-V/Si laser source



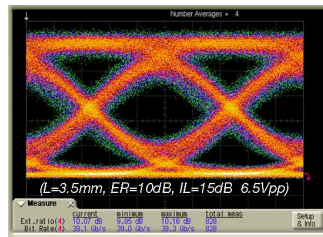
Preliminary results:
 $I_{th} < 30\text{mA}$, $P > 3\text{dB}_m$, CW operation

Main results (2)

- Silicon based modulators at 10Gb/s⁽¹⁾ and 40Gb/s⁽²⁾



390nm SOI
ER = 8.1 dB, IL= 6 dB @10Gb/s

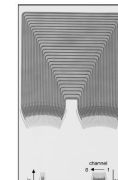
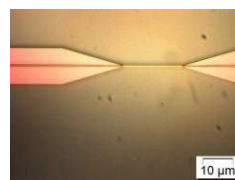
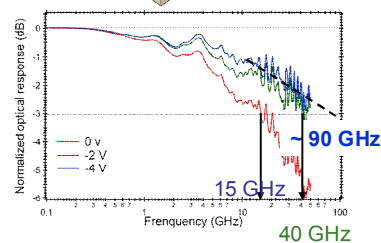
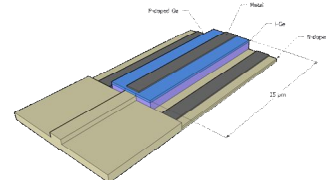


220nm SOI
ER = 10 dB, IL= 15 dB @40Gb/s

⁽¹⁾ Gilles Rasigade et al., "High extinction ratio 10 Gbit/s silicon optical modulator," Opt. Express 19, 5827-5832 (2011)
⁽²⁾ D. J. Thomson et al., "High contrast 40Gbit/s optical modulation in silicon," Opt. Express 19, 11507-11516 (2011)

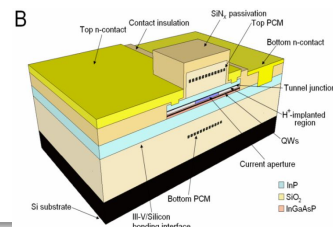
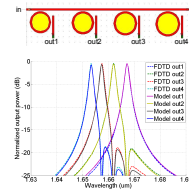
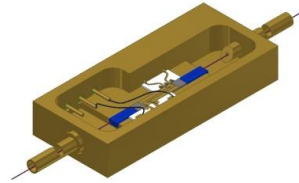
Main results (3)

- Demonstration of high responsivity (0.8-1A/W), low dark current and high BW photodiodes
- Efficient passive waveguides (Mux/Demux, polarization diversity circuit, fiber coupling, rib/strip transition)

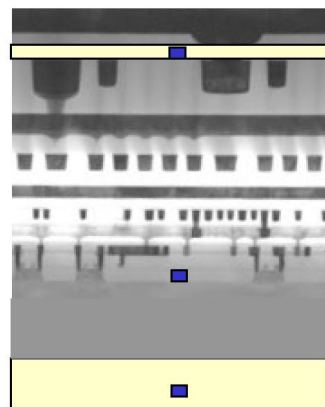


Main results (4)

- Investigation of generic packaging solutions
- Establishment of a photonics design flow
- Investigation of novel concepts for light emission and modulation



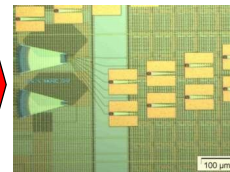
Photonics integration options



Option 1
Photonic layer at the last levels of metallizations with back-end fabrication

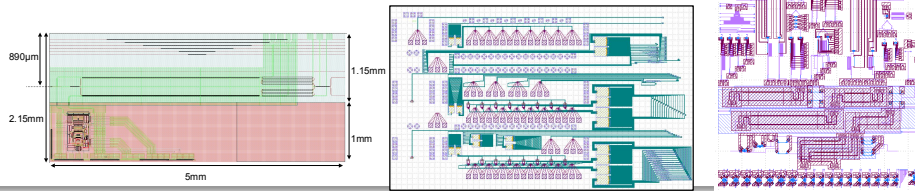
Option 2
Combined front-end fabrication

Option 3
Backside fabrication



Conclusion

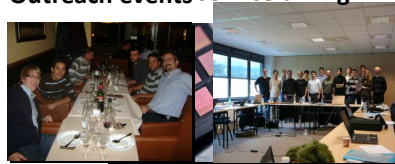
- HELIOS has developed a full design, fabrication and integration chain that could be used for many applications
- Demonstrators are now under fabrication
 - Integrated modulator + driver
 - WDM transceivers
 - QAM-10Gbps wireless transmission systems



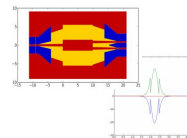
What is ePIXfab ?

Access to silicon photonics technology for academic and industry R&D

Outreach events **MRM** service **Training**



CAD



Transfer to production



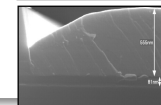
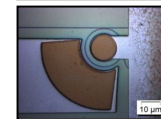
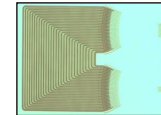
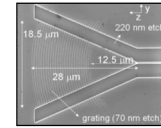
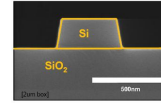
Partially funded by the EC



www.epixnet.org
www.photonfab.eu

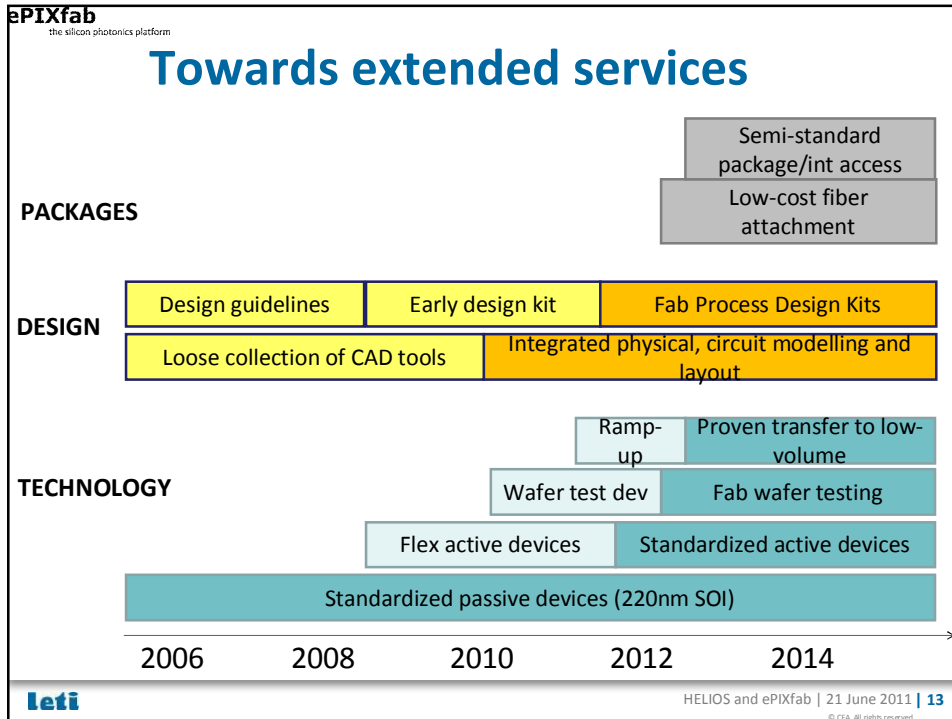
MPW shuttle service

- 3-5 shuttles per year based on 2 technology providers
 - Imec:
 - 200mm wafer fab, ~0.13um technology, industrial tooling
 - 2-layer and 4-layer passive device processes
 - Edge couplers (Ugent)
 - 2012: modulators & heaters
 - CEA-LETI:
 - 200mm wafer fab, ~0.13um technology , industrial tooling
 - 2 layer passive device process
 - Thermo-optic heaters
 - + Flexible access to implants, contacts, Ge epitaxy, metalization
 - photodetectors and modulators



What's up next?

- Maturity of design flow and technology
- Standardized active/passive integration
- Access to packaging & integration services
- Focus on SMEs
- Single point of access to a larger consortium of Si photonics expertise centers



- ePIXfab**
the silicon photonics platform
- ## Packaging
1. Low-cost fiber attachment and wirebonding
 - Test chips in a testbed/lab
 - ~10-20 chips
 - Not manufacturable, just for chip testing
 2. Semi-standardized package approaches
 - Use chips in demonstrators and prototypes
 - Few chips
 - Path to manufacturing
 - Access to packaging, integration, testing expertise
- let** HELIOS and ePIXfab | 21 June 2011 | 14
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Testing

- (Semi-)automated wafer testing being deployed at fabs (CEA-LETI, Imec)
- Some agreement on process & device benchmarks and test procedures needed (e.g.: waveguide performance, modulator performance, ...)



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**Thanks for
your attention**

